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# RELIABLE SOLID-STATE CIRCUITS

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# I. Introduction

Electronic systems designed for space-age utilization must be highly efficient, small in size, and very reliable. An important application that appears likely to satisfy all three requirements is the use of pulse-width modulation for linear power amplification. Preliminary work in this area has been reported in Semiannual Report No. 1 [15]. During the second six-month period of grant research, covered by this report, attention has been focused on the development of a novel approach to PWM, compatible with the design constraints imposed by microcircuit realization. This approach shows great promise for technological utilization.

The use of pulse-width modulation for linear power amplification has been known for many years [1, 2]. The advantages of such techniques are the high efficiency inherent in their use and the fact that, since individual stages act as switches, performance is not degraded unless switching transistions are actually inhibited. On the other hand, the maximum theoretical efficiency of a conventional class B design is 78%, while in practice a value of 50% is typical. In addition, the active devices used in conventional designs must be operated within their linear ranges. Hence, performance may be quite sensitive to environmental changes and component aging.

The availability of semiconductor devices, with their low collector-leakage current in the "off" condition, and their low saturation voltage in the "on" condition, increases the potential advantage of PWM techniques and makes their use even more attractive. A number of articles have appeared recently extolling the virtues of PWM for the audiophile [3-8]. Applications for commercial and aerospace electronics systems have been fewer [9-14], but indicate a growing interest.

In Chapter II, an approach to the design of a pulse-width modulator is presented. It should be emphasized that although particular circuits are discussed, the methods are applicable to a variety of circuits and devices having open-circuit stable negative-resistance characteristics. Chapter III discusses the design of a pulse-power stage to best utilize the advantages of a switching amplifier, while Chapter IV describes an audio power -amplifier application. The circuits presented here have been designed to meet requirements for microminiaturization.

In addition to the work on switching amplifiers, research during this report period has continued in the area of reliability theory, with emphasis on an analytical formulation of reliability improvement through specific redundant configurations. This method may be applied not only to simple arrays of components, such as resistors and capacitors, but to arrays of solar cells and amplifiers as well. Although the

configurations considered are limited to series-parellel composites, it is hoped that the techniques may be extended to a more general topology. This work is presented in Chapter V.

## II. A Linear Pulse-Width Modulator

In this chapter a design for a linear pulse-width modulator is presented and analyzed. This design has the following desirable features:

(1) Simple, free-running concept,

(2) High degree of linearity,

(3) Ease of microminiaturization.

The basic modulator circuit, shown in Fig. 2.1, if operated with one capacitor between terminals 1-2 (as in Fig. 2.1(a)), produces a linear, variable-frequency PWM output when current sources $I_1$ and $I_2$ are modulated by an input signal. A linear, constant-frequency PWM output may be obtained using either of the switched capacitor networks shown in Fig. 2.1(b) and (c), if voltage sources $V_1$ and $V_2$ are modulated by the input signal.

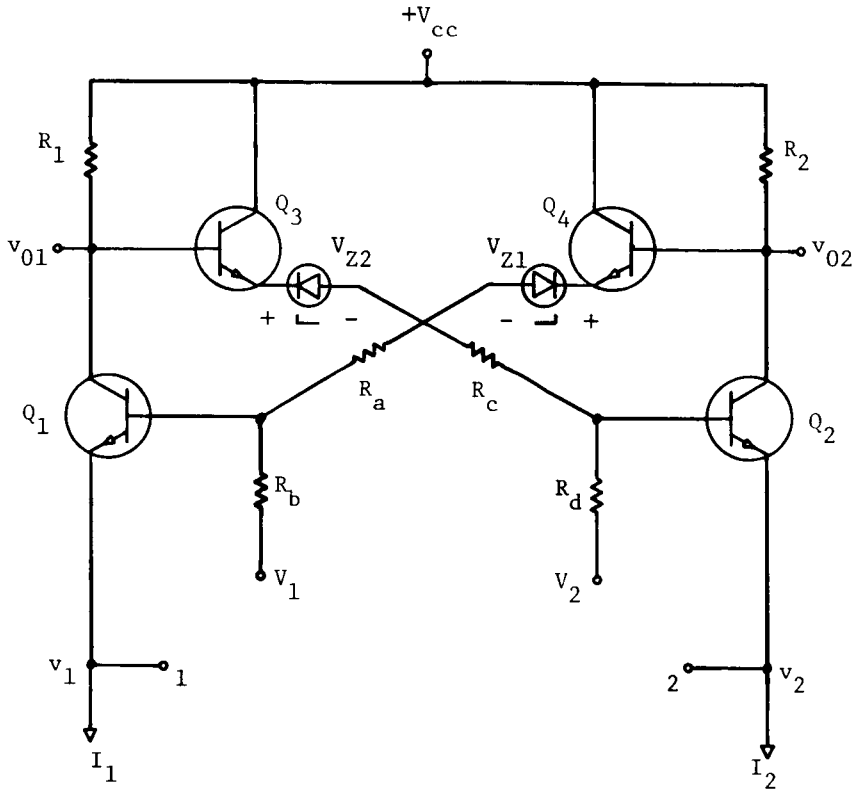
In the circuit of Fig. 2.1, collector resistors ($R_1$, $R_2$), zener voltages ($V_{Z1}$, $V_{Z2}$) and cross-coupling voltage-divider ratios (formed by $R_a$, $R_b$ and $R_c$, $R_d$) are assumed to be different so that performance sensitivity to these parameters may be investigated in the analysis that follows. To simplify notation without loss of generality, all transistor base-emitter drops ($V_{be}$) are considered to be equal. Any differences in $V_{be}$ drops could be included in $V_{Z1}$ and $V_{Z2}$. It is assumed that the output impedance of emmiter followers $Q_3$ and $Q_4$ is very low compared to resistors $R_a$ and $R_c$ and that the input impedance of switching transistors $Q_1$ and $Q_2$ is high compared to resistors $R_b$ and $R_d$. Also, the sum of the currents $I_1$ and $I_2$ must be constant and equal to I.

Free-running switching operation of the circuit (illustrated by the $Q_2$ collector waveform shown in Fig. 2.2(a)) is obtained with any one of the capacitor networks (a), (b), or (c). Now, if $Q_1$ is on while $Q_2$ is off, $Q_1$ carries the total current I and emitter-voltage $v_1$ is clamped to $v_{1C}$, which is given by

$$v_{1C} = a_1(V_{cc} - V_{be} - V_{Z1} + b_1V_1) - V_{be} \quad , \qquad (2.1)$$

where $a_1 = R_b/(R_a + R_b)$ and $b_1 = R_a/R_b$. During this interval ($0<t<T_1$), $v_2$ decreases while capacitor C is being charged by current $I_2$. Switching occurs when $v_2$ has come to within one base-emitter drop of the voltage at the base of $Q_2$. The $v_2$ switching level ($v_{2S}$) is given by

$$v_{2S} = a_2(V_{cc} - V_{be} - V_{Z2} + b_2V_2 - IR_1) - V_{be} \quad , \qquad (2.2)$$



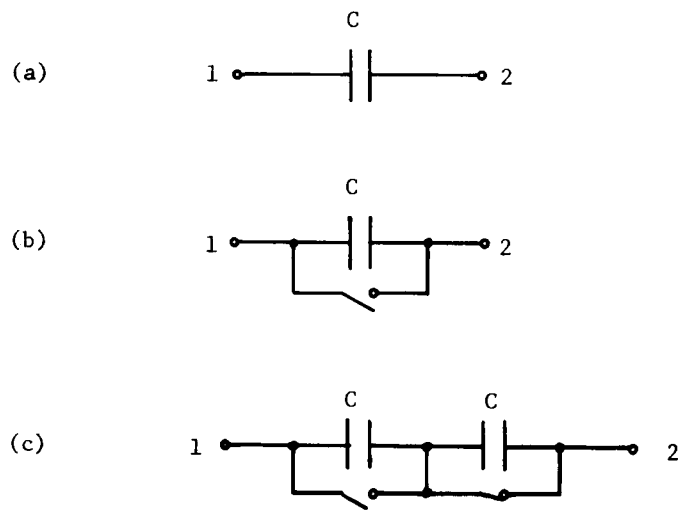




Fig. 2.1 Basic linear modulator circuit: (a) capacitor network for variable-frequency operation; capacitor networks for constant-frequency operation, (b) momentary switch and, (c) alternating switch.

where $a_2 = R_d/(R_c + R_d)$ and $b_2 = R_c/R_d$. At this instant ($t = T_1$), $Q_2$ should turn on and $Q_1$ must turn off. During the next interval ($T_1<t<(T_1+T_2)$), $Q_2$ carries the total current I, $v_2$ is clamped to

$$v_{2C} = a_2(V_{cc} - V_{be} - V_{Z2} + b_2V_2) - V_{be} \quad , \qquad (2.3)$$

and $v_1$ decreases while capacitor C is charged (in the opposite direction) by current $I_1$. The next switching transition occurs at $t = T_1 + T_2$, when $v_1$ has come to within $V_{be}$ of the voltage at the base of $Q_1$. This switching level is given by

$$v_{1S} = a_1(V_{cc} - V_{be} - V_{Z1} + b_1V_1 - IR_2) - V_{be} \quad . \qquad (2.4)$$

For oscillation to be sustained (with period $T = T_1 + T_2$), the voltage swing at collectors $Q_1$ and $Q_2$ must be sufficient to drive the opposite transistor into cut-off. Operation as a linear modulator, however, requires that the voltage swing be limited to avoid saturation of $Q_1$ or $Q_2$. The voltage constraint necessary to keep $Q_1$ out of saturation is

$$V_{cc} - IR_1 \geq a_1(V_{cc} - V_{be} - V_{Z1} + b_1V_1) \quad , \qquad (2.5)$$

while the corresponding constraint for $Q_2$ is

$$V_{cc} - IR_2 \geq a_2(V_{cc} - V_{be} - V_{Z2} + b_2V_2) \quad . \qquad (2.6)$$

These constraint relations will be used to determine the proper zener voltages and/or divider ratios to maximize the output voltage swing of the modulator for linear operation.

2.1 Linear, variable-frequency operation.

With the simple capacitor network shown in Fig. 2.1(a) connected between terminals 1-2, circuit performance is characterized by a decrease in switching frequency as modulation level is increased. For many applications this is not a problem, while the simplicity of the circuit and linearity of the modulation process are very attractive.

Operation of the circuit is best understood with the help of the waveforms for $v_1$, $v_2$ and $v_C$ shown in Fig. 2.2, where $v_C$ is the voltage across capacitor C and

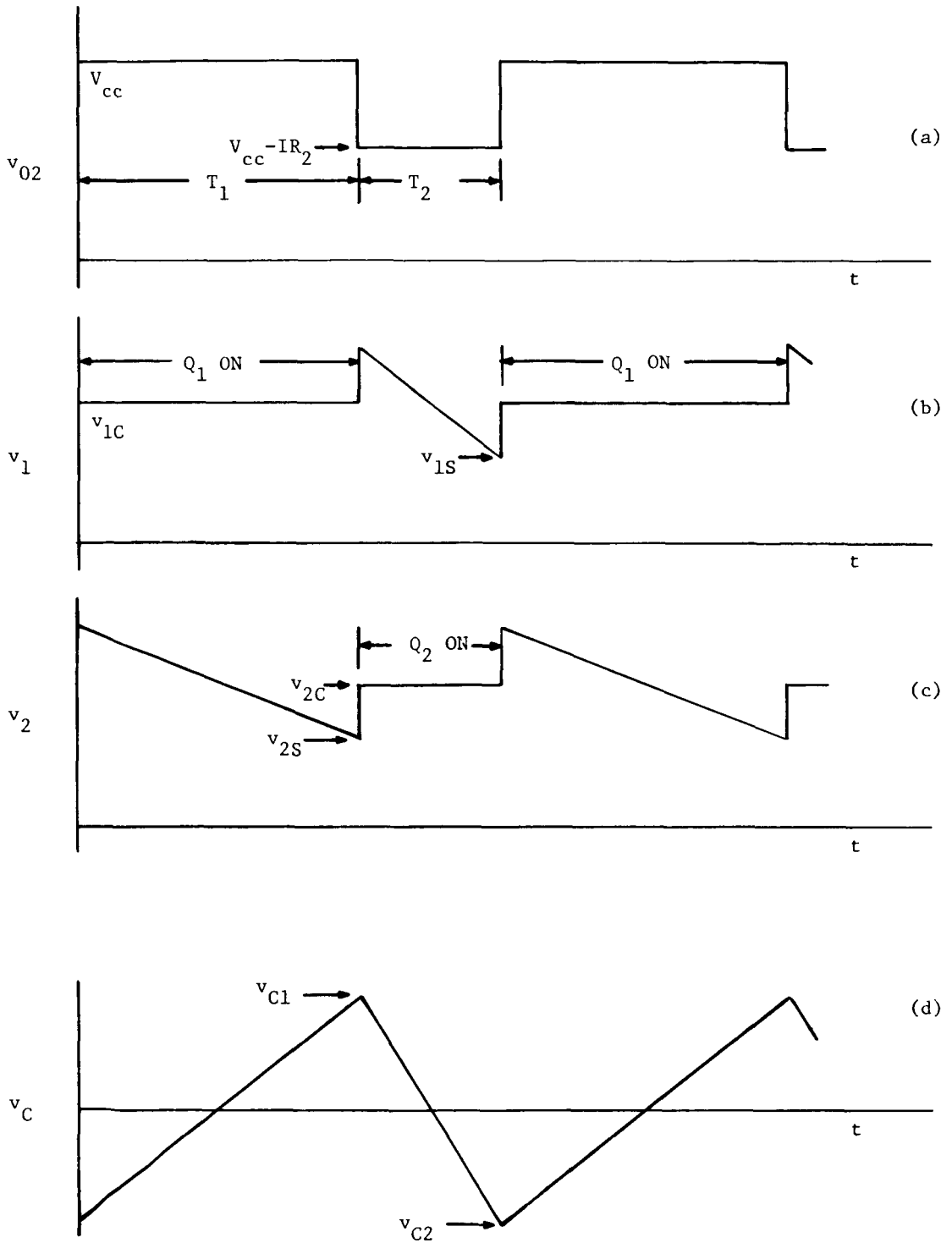



Fig. 2.2 Modulator voltage waveforms for variable-frequency operation: (a) $Q_2$ collector; (b) $Q_1$ emitter; (c) $Q_2$ emitter; (d) capacitor network.

is taken to be

$$v_C = v_1 - v_2 \quad . \tag{2.7}$$

It can be seen from these waveforms that the maximum capacitor voltage $v_{C1}$ must be given by the difference between $v_1$ and $v_2$ just before switching takes place at $t = T_1$. This value is

$$v_{C1} = v_{1C} - v_{2S} \quad . \tag{2.8}$$

The minimum capacitor voltage $v_{C2}$ exists at $t = T_1 + T_2$ and is given by

$$v_{C2} = v_{1S} - v_{2C} \quad . \tag{2.9}$$

It is obvious that the capacitor voltage swing during each charging interval is the same, and, by use of (2.1), (2.2), (2.3), and (2.4) with (2.8) and (2.9), this value is found to be

$$\Delta v_C = v_{C1} - v_{C2} = I(a_1R_2 + a_2R_1) \quad . \tag{2.10}$$

It should be observed that the pulse lengths $T_1$ and $T_2$ can be modulated only by current sources $I_1$ and $I_2$ in this version of the circuit. Hence, $V_1$ and $V_2$ may be one common voltage-reference point. Now, let $I_1 = (1 + m)I/2$ and $I_2 = (1 - m)I/2$, where m is the modulation level ($-1 \leq m \leq 1$). Since $I_2$ charges the capacitor at a constant rate during $0<t<T_1$, then, upon substitution from (2.10),

$$T_1 = C\Delta v_C/I_2 = 2C(a_1R_2 + a_2R_1)/(1 - m) \quad , \tag{2.11}$$

In similar fashion, since $I_1$ charges the capacitor during $T_1<t<(T_1+T_2)$,

$$T_2 = C\Delta v_C/I_1 = 2C(a_1R_2 + a_2R_1)/(1 + m) \quad . \tag{2.12}$$

The resulting pulse-width modulation process is linear as can be demonstrated by taking the average value of the output waveform at the collector of $Q_2$ (shown in Fig. 2.2(a))

$$\bar{v}_{02} = [T_1V_{cc} + T_2(V_{cc} - IR_2)]/(T_1 + T_2) \quad . \tag{2.13}$$

Substitution from (2.11) and (2.12) into (2.13) yields

$$\bar{v}_{02} = (V_{cc} - IR_2/2) + mIR_2/2 \quad , \qquad (2.14)$$

which is a linear function of m. The complement appears at the collector of $Q_1$ and is given by

$$\bar{v}_{01} = (V_{cc} - IR_1/2) - mIR_1/2 \quad . \qquad (2.15)$$

The effect of modulation level on switching frequency f is found by substituting (2.11) and (2.12) into

$$f = 1/T = 1/(T_1 + T_2) \quad , \qquad (2.16)$$

which results in

$$f = (1 - m^2)[1/4C(a_1R_2 + a_2R_1)] \quad . \qquad (2.17)$$

The zero-signal switching frequency is found from (2.17) with m = 0. Hence,

$$f_0 = 1/4C(a_1R_2 + a_2R_1) \quad . \qquad (2.18)$$

It should be noted by examination of (2.14), (2.15) and (2.17) that the modulation process is not sensitive to zener or base-emitter drops, or divider ratios, although the switching frequency is a function of $a_1$ and $a_2$ and modulation level. The linearity of the modulation process depends primarily on the current sources $I_1$ and $I_2$ and how well they track the modulating signal. Also, in order to operate with a high modulation level, $f_0$ should be typically about ten times the highest frequency contained in the spectrum of the input signal. For example, if m = .9 and $f_0$ = 100 kc, the switching frequency is only 19 kc. Under these conditions, spurious harmonics might affect the performance of a PWM audio amplifier.*

For practical realization of the circuit, assume that $R_1 = R_2 = R$, $a_1 = a_2 = a$, $b_1 = b_2 = b$, $V_1 = V_2 = V$, and that $V_{Z1} = V_{Z2} = V_Z$. Now, suppose that the design of the current source requires that voltage levels at the emitter of $Q_1$ and $Q_2$ not fall below a certain minimum level $V_E$. From Fig. 2.2(b) and (c), it is seen that

*See discussion and references cited in Chapter IV.

this requirement leads to the constraint

$$V_E \leq v_{1S} = v_{2S} = a(V_{cc} - V_{be} - V_Z + bV - IR) - V_{be} \quad . \qquad (2.19)$$

From (2.5) or (2.6) the saturation constraint is

$$V_{cc} - IR \geq a(V_{cc} - V_{be} - V_Z + bV) \quad . \qquad (2.20)$$

In order to realize the constraints of (2.19) and (2.20) it is not necessary to utilize both zener diodes and voltage dividers in the network. If, for example, it is desired to use the divider network, let $V_Z = V = 0$. Use of the constraint equalities included in (2.19), (2.20) and solution of these equations for the proper values of a and R yields

$$a = [V_{be}/2(V_{cc} - V_{be})][1 + 4(V_E + V_{be})(V_{cc} - V_{be})/V_{be}^2]^{1/2} \quad , \qquad (2.21)$$

$$R = [V_{cc}(1 - a) + aV_{be}]/I \quad . \qquad (2.22)$$

A circuit designed for $V_E = +2$ volts, $V_{cc} = 12$ volts and $I = 1.5$ ma., employing a differential amplifier for modulation, is shown in Fig. 2.3 . The constraints are satisfied for $a = 1/2$ and $R = 4.7$ KΩ. A variation of .25 volts above and below ground fully modulates the output. The zero-signal switching frequency is 100 kc. An experimentally determined transfer characteristic (normalized) and a plot of switching frequency versus modulation level for this circuit are shown in Fig. 2.4 . Deviation of the output from linearity at high input levels is due primarily to the current source. For a sinusiodal input to the modulator, less than 2.4% harmonic distortion is obtained at a peak modulation level of $m = .9$ . As can be observed, the switching-frequency curve is close to the parabolic shape indicated by (2.17).

If circuit realization using zeners is preferred, then we can set $R_a = R_c = 0$, which gives $a = 1$, $b = 0$. In this case, solution of the equalities given in (2.19) and (2.20) yield design values for $V_Z$ and R that are

$$V_Z = (V_{cc} - 3V_{be} - V_E)/2 \quad , \qquad (2.23)$$

$$R = (V_Z + V_{be})/I \quad . \qquad (2.24)$$

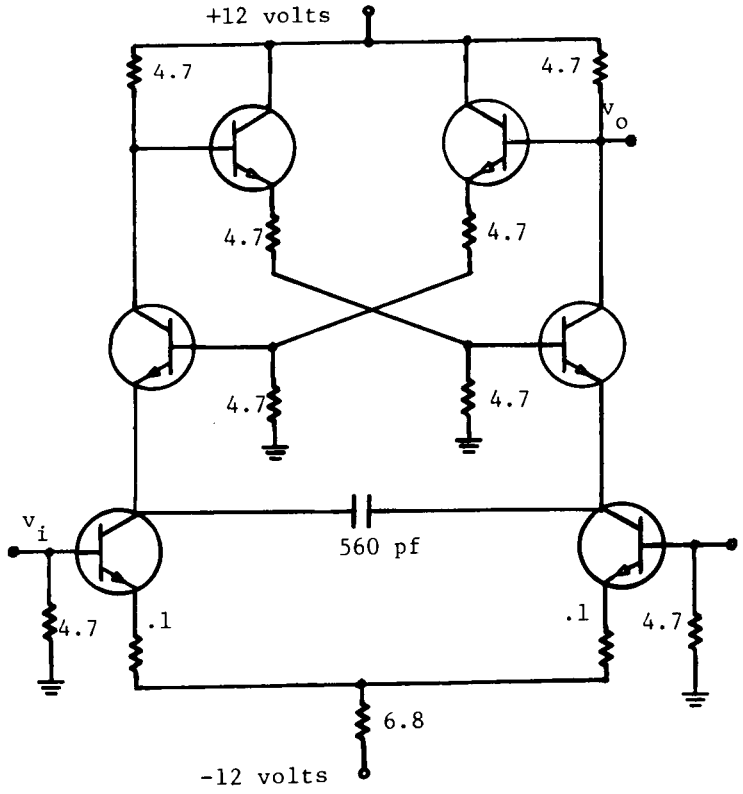



Fig. 2.3 Practical linear modulator circuit for variable-frequency operation. Note: (1) all transistors 2N706; (2) all resistors in kilohms.

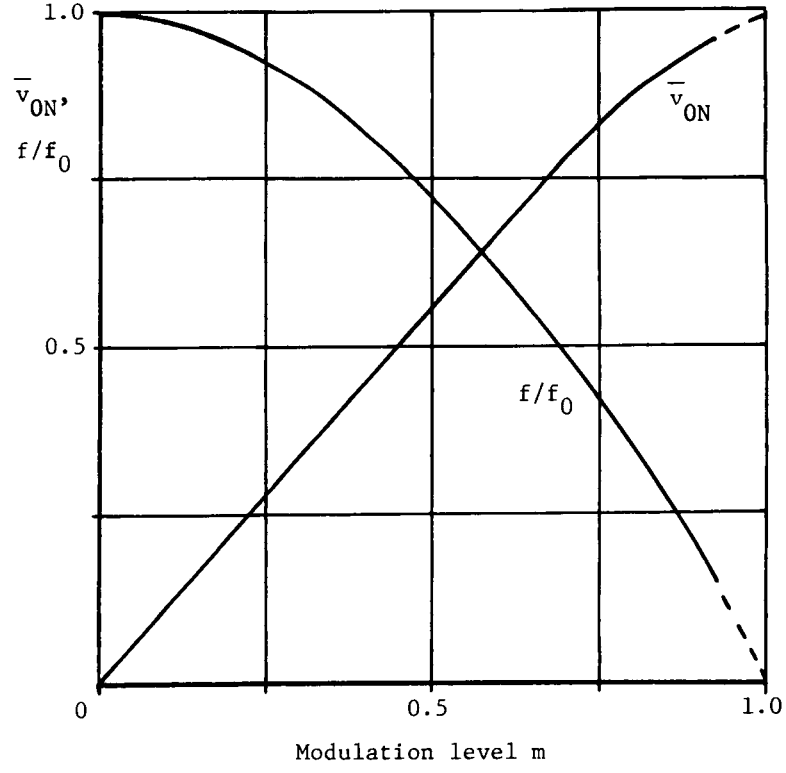



Fig. 2.4 Curves of normalized switching frequency, $f/f_0$, and normalized average output, $\overline{v}_{ON}$, versus input modulation level m, for the linear, variable-frequency PWM design.

With zener operation the zero-signal switching frequency is found from (2.18) to be

$$f_0 = 1/8RC \quad , \qquad (2.25)$$

which allows a smaller capacitor to be used for a given $f_0$, compared with the previous realization. This may be an important consideration when designing in integrated form.

An important circuit simplification is possible if a complementary output is not necessary. In this case, if $R_1 = 0$ and $R_2 = R$, one cross-coupling network can be eliminated entirely, while the other may be directly coupled, as shown in Fig. 2.5 . Saturation is just avoided in $Q_2$ if the bias at the base of $Q_2$ is set so that

$$V_B = V_{cc} - IR \quad , \qquad (2.26)$$

where R is determined by the constraint for $V_E$ in (2.19), which becomes for the simplified circuit,

$$V_E \leq V_{cc} - IR - V_{be} \quad . \qquad (2.27)$$

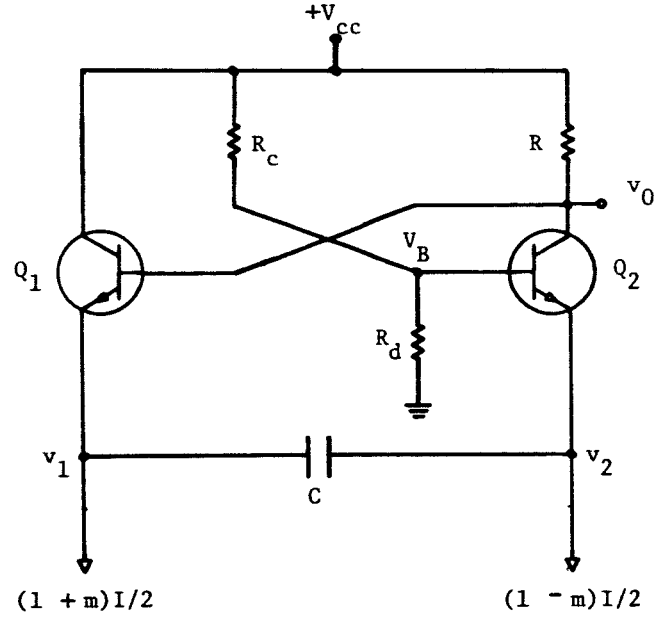



Fig. 2.5 Simplified linear variable-frequency modulator

The value of R that realizes the maximum collector-voltage swing is, therefore,

$$R = (V_{cc} - V_{be} - V_E)/I \quad , \qquad (2.28)$$

and the zero-signal switching frequency is, from (2.18),

$$f_0 = 1/4RC \quad . \qquad (2.29)$$

This circuit has been constructed and performance has been found to equal that of the balanced modulator described previously. Its application in a PWM audio power system will be discussed in Chapter IV.

2.2 Linear, constant-frequency operation.

As has already been pointed out, the use of a single capacitor with the circuit of Fig. 2.1 produces a linear PWM output with a switching frequency that decreases with the square of the modulation level. This performance arises because the pulse lengths are varied by modulating the charging currents which appear in the denominators of (2.11) and (2.12). If, however, the charging currents are held constant and the modulation of $\Delta v_C$ in (2.11) and (2.12) is made proportional to m, the period should be insensitive to modulation level.

Thus, in order to produce linear pulse-width modulation with constant switching frequency from the basic circuit of Fig. 2.1, the current sources are set so that $I_1 = I_2 = I/2$ and voltage sources $V_1$ and $V_2$ are modulated so that $V_1 = V_b + mV$ and $V_2 = V_b - mV$, where $V_b$ is the bias necessary for free-running operation, and V is the maximum signal voltage. To make constant-frequency operation possible, however, the timing capacitor must be discharged (ideally to zero) at the beginning of each switching interval. The network shown in Fig. 2.1(b), where the switch closes momentarily at the beginning of each interval, and the network shown in Fig. 2.1(c), where the switches alternate at each interval, are both suitable for this purpose. However, practical realization of such a network requires the use of diodes or transistors to steer the charging current and provide a discharge path for the capacitor. Therefore, the equivalent circuit of a practical capacitor-switching network to be used in the following analysis, includes diode drops ($V_{d1}$, $V_{d2}$) and discharge voltages ($v_{D1}$, $v_{D2}$). In this equivalent circuit, shown in Fig. 2.6, when the charging current is toward the right, the switches are in positions S1, and capacitor $C_1$ charges from initial value $v_{D1}$ until the current reverses, at which time the switches change to contacts S2 and capacitor $C_2$ charges in the opposite direction from an initial value $v_{D2}$. Switching operation is illustrated by the waveforms shown in Fig. 2.7, where, as before,

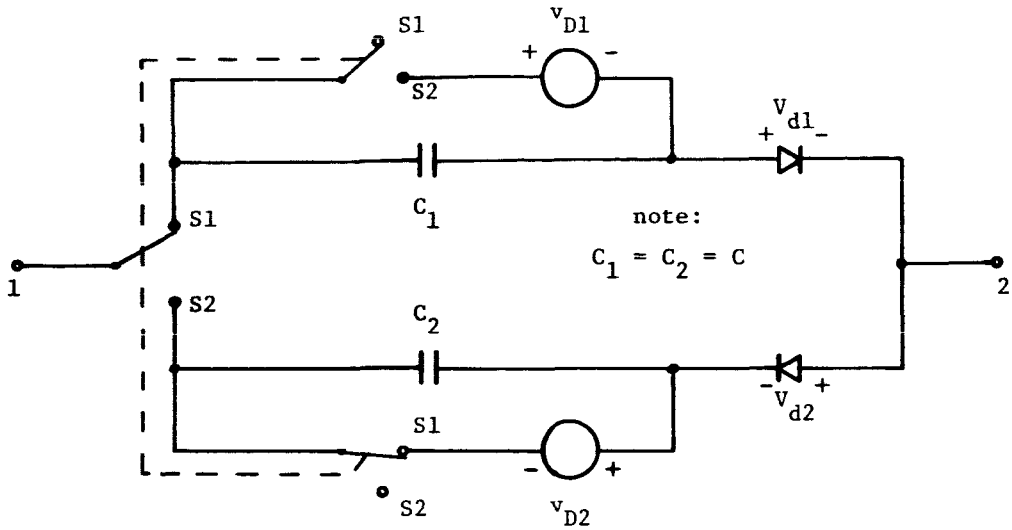



Fig. 2.6 Equivalent circuit of capacitor switching network for constant-frequency operation.

$v_C$ is the voltage appearing between terminals 1-2 of Fig. 2.1 . Hence,

$$v_{C1} = v_{1C} - v_{2S} \quad ; \tag{2.30}$$

$$v_{C2} = v_{1S} - v_{2C} \quad . \tag{2.31}$$

Now, with modulation of $V_1$ and $V_2$ as defined previously, and with $a_1 = a_2 = a$, $b_1 = b_2 = b$, $V_{Z1} = V_{Z2} = V_Z$, substitution of (2.1), (2.2), (2.3), and (2.4) into (2.30) and (2.31) yields

$$v_{C1} = a(IR_1 + 2bmV) \quad ; \tag{2.32}$$

$$v_{C2} = -a(IR_2 - 2bmV) \quad . \tag{2.33}$$

The capacitor voltage swing $\Delta v$, during successive intervals must be less than the magnitude of $v_{C1}$ or $v_{C2}$ by the series voltage drop and the initial (discharge) voltage. Therefore, at time $t = T_1$,

$$\Delta v_1 = a(IR_1 + 2bmV) - (v_{D1} + V_{dL}) \quad , \tag{2.34}$$

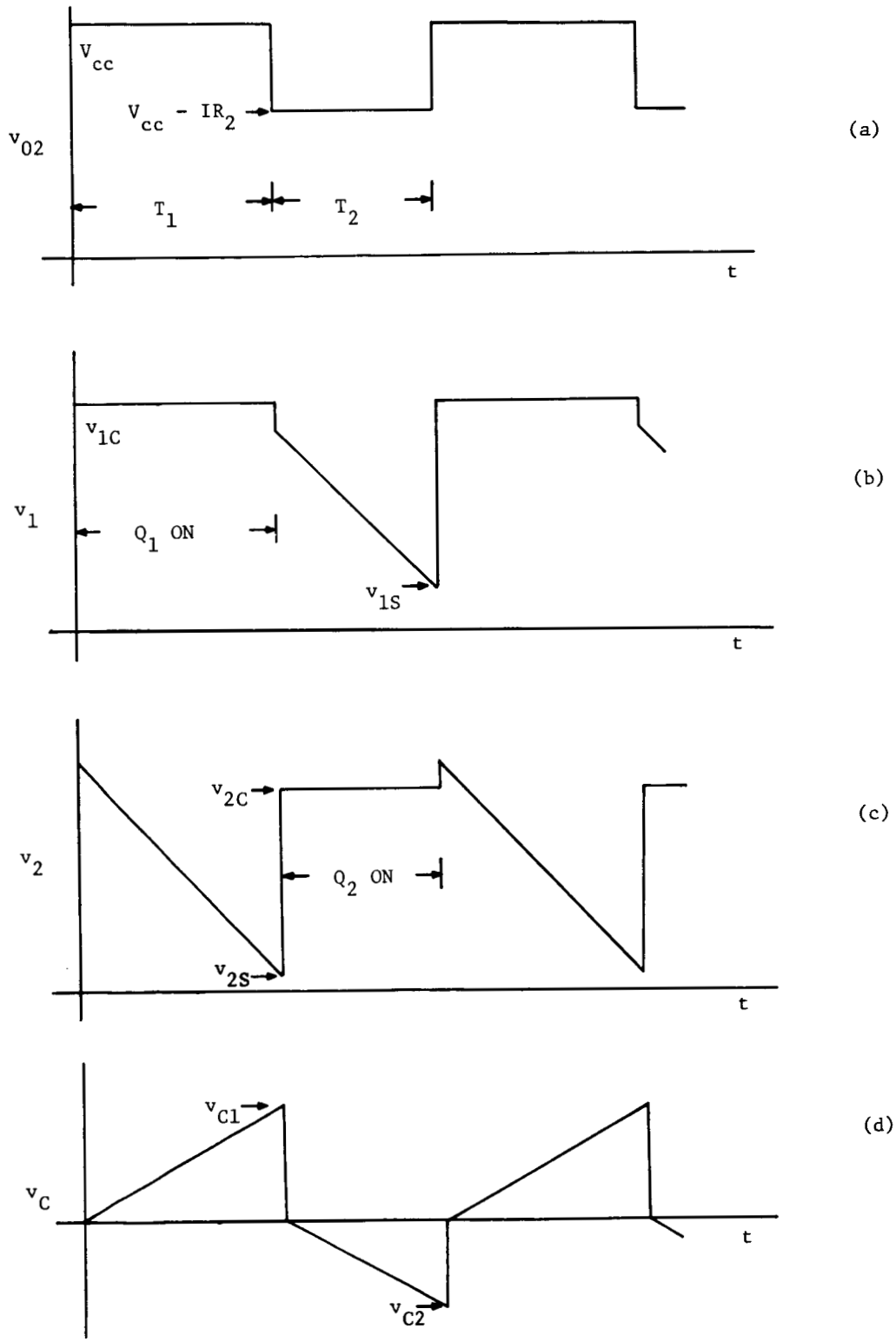



Fig. 2.7 Modulator voltage waveforms for constant-frequency operation: (a) $Q_2$ collector; (b) $Q_1$ emitter; (c) $Q_2$ emitter, and (d) capacitor network.

and, at time $t = T_1 + T_2$,

$$\Delta v_2 = a(IR_2 - 2bmV) - (v_{D2} + V_{d2}) \quad . \qquad (2.35)$$

Since the charging currents are both equal to I/2, the pulse lengths as determined from (2.34) and (2.35) are

$$T_1 = 2C[a(IR_1 + 2bmV) - (v_{D1} + V_{d1})]/I \quad ; \qquad (2.36)$$

$$T_2 = 2C[a(IR_2 - 2bmV) - (v_{D2} + V_{d2})]/I \quad . \qquad (2.37)$$

Addition of these pulse lengths yields an expression for the switching period

$$T = 2C[aI(R_1 + R_2) - (v_{D1} + v_{D2}) - (V_{d1} + V_{d2})]/I \quad , \qquad (2.38)$$

which is independent of m, if initial voltages $v_{D1}$, $v_{D2}$ are independent of m. If this is true, then, to simplify notation, let $v_{D1} = v_{D2} = V_o$, $V_{d1} = V_{d2} = V_d$, and $R_1 = R_2 = R$. For these conditions, it can be seen from (2.36) or (2.37) that in order to realize full modulation ($m = \pm 1$), one of the design constraints must be

$$2abV = aIR - (V_o + V_d) \quad . \qquad (2.39)$$

Using this constraint in the expressions for $T_1$ and $T_2$ from (2.36) and (2.37), we obtain

$$T_1 = 2aRC[1 - (V_o + V_d)/aIR](1 + m) \quad ; \qquad (2.40)$$

$$T_2 = 2aRC[1 - (V_o + V_d)/aIR](1 - m) \quad , \qquad (2.41)$$

and the switching frequency

$$f = 1/4aRC[1 - (V_o + V_d)/aIR] \quad . \qquad (2.42)$$

It can easily be shown from (2.30) and (2.31) in the general case, that $T_1$ and $T_2$ are sensitive to changes in zener voltages or divider ratios in such a way as to increase one and decrease the other while the period remains constant. In contrast to this effect, corresponding values of $T_1$ and $T_2$ found for the variable-frequency design were shown not to be sensitive at all to voltage changes, while divider-ratio changes affected both lengths by the same factor, resulting only in a change in overall period. Pulse-length sensitivity to component changes seems to be the price that

must be paid to achieve constant-frequency operation.

That the modulation process is linear with m may again be demonstrated by taking the average value of the output waveform at $Q_2$, given by (2.13), and substituting for $T_1$ and $T_2$ from (2.40) and (2.41). Thus,

$$\overline{v}_{02} = (V_{cc} - IR/2) + mIR/2 \quad . \tag{2.43}$$

The complement appears at the collector of $Q_1$ and is given by

$$\overline{v}_{01} = (V_{cc} - IR/2) - mIR/2 \quad . \tag{2.44}$$

The saturation constraint and the $Q_1$, $Q_2$ emitter voltage constraint, determined from (2.2), (2.3), (2.4), (2.5) and (2.6), with $m = \pm 1$ (worst case) are

$$V_{cc} - IR \geq a[V_{cc} - V_{be} - V_Z + b(V_b + V)] \quad ; \tag{2.45}$$

$$V_E + V_{be} \leq a[V_{cc} - V_{be} - V_Z + b(V_b - V) - IR] \quad . \tag{2.46}$$

A much-simplified version of the constant-frequency circuit can be realized if it is not necessary to provide a complementary output. This circuit, shown in Fig. 2.8 is quite similar to the corresponding variable-frequency design. The modulation signal is applied directly to the base of $Q_2$. The zener diode is necessary to meet the saturation constraint

$$V_b + V \leq V_{cc} - IR \quad , \tag{2.47}$$

while permitting full modulation to be achieved when $m = \pm 1$. Use of the equality included in (2.47), and the condition that $T_1 = T_2$ for $m = 0$, results in

$$T_1 = RC[1 - 2(V_o + V_d)/IR](1 + m) \quad ; \tag{2.48}$$

$$T_2 = RC[1 - 2(V_o + V_d)/IR](1 - m) \quad ; \tag{2.49}$$

$$f = 1/2RC[1 - 2(V_o + V_d)/IR] \quad . \tag{2.50}$$

Also, the necessary IR drop and zener voltage are given by

$$IR = 2(V + V_o + V_d) \quad , \tag{2.51}$$

and

$$V_Z = IR - (V_o + V_d) \quad . \qquad (2.52)$$

Now, if a constraint is placed on the minimum voltage at the emitter of $Q_1$, then V must be chosen such that

$$V \leq [V_{cc} - V_E - V_{be} - 3(V_o + V_d)]/4 \quad . \qquad (2.53)$$

2.3 Capacitor switching networks.

Capacitor switching networks suitable for use with the circuit of Fig. 2.1 in the constant-frequency mode of operation are shown in Fig. 2.9 . In each network, a timing capacitor is discharged at the beginning of a switching interval. For example, in the network of Fig. 2.9(a), if the current starts toward the right, transistor $Q_2$ discharges $C_2$ and then saturates while $C_1$ charges; when the current reverses, $Q_1$ discharges $C_1$, and $C_2$ charges. For this circuit, the level to which each capacitor is discharged is equal to the saturated collector-emitter voltage of the discharge transistor, and each capacitor charges through a base-emitter junction which causes a

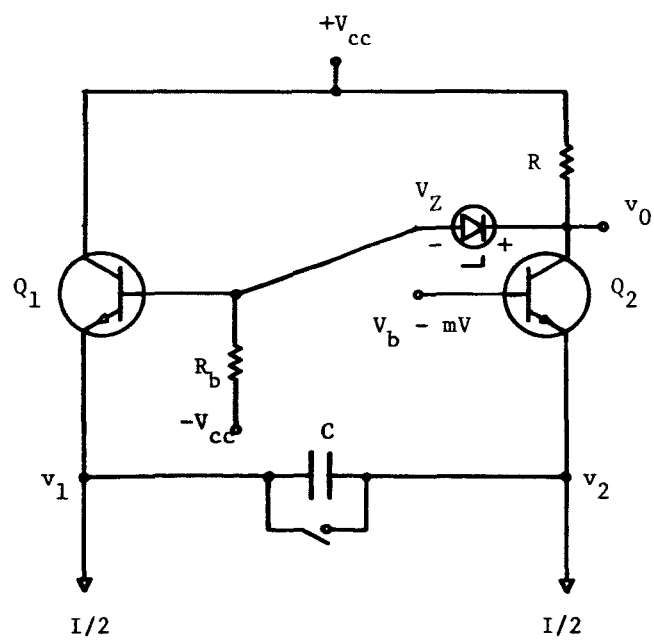



Fig. 2.8 Simplified linear constant-frequency modulator.

voltage drop in series with the charging current. The two-capacitor network, therefore, may be represented by the equivalent circuit of Fig. 2.6 and its performance described by the analysis of the preceding section.

It should be noticed that in the two-capacitor network, the discharge voltage across the timing capacitor at the beginning of a switching interval ($v_{D1}$ or $v_{D2}$) is always the same polarity as the voltage to which it charges at the end of the interval. Furthermore, the voltage at the end of the interval, just before the instant of switching, is greater than the discharge level $V_o$ (in this case, $V_o = V_{CE(sat)}$).

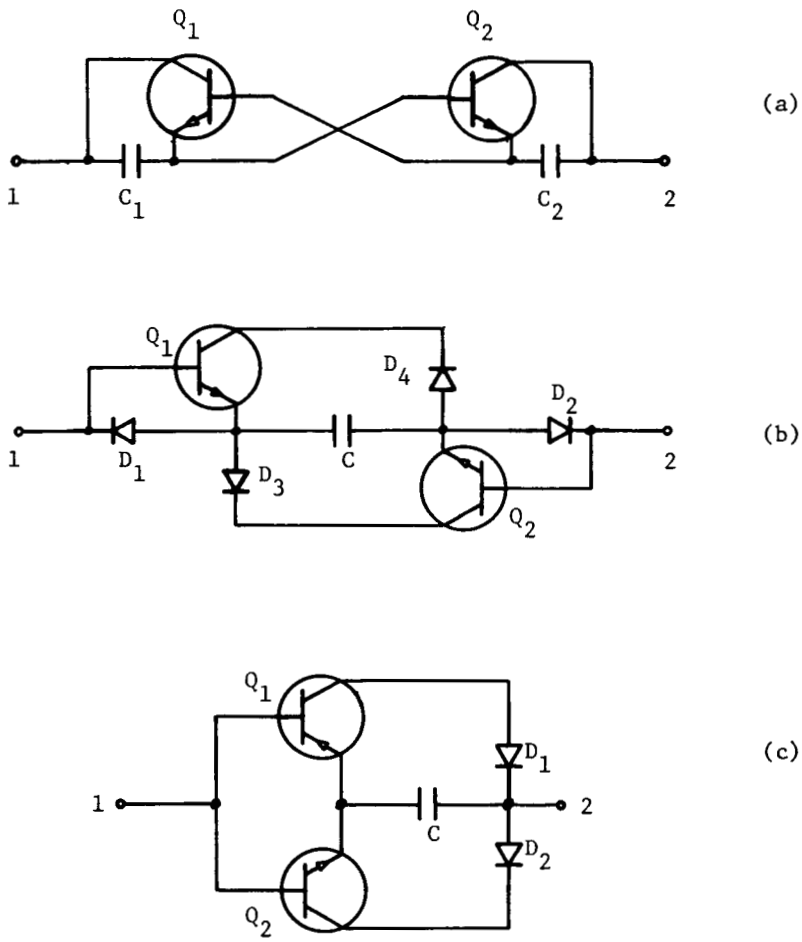



Fig. 2.9 Capacitor switching networks for practical realization of constant-frequency operation.

This is not the case, however, for the single-capacitor networks shown in Fig. 2.9(b) and (c), since the voltage at the end of an interval may not be sufficient to establish the proper discharge level at the beginning of the next interval. This fact causes an increase in switching frequency at high modulation levels, with a corresponding nonlinearity in the modulation process. An analysis of this effect is included in the following discussion of the single-capacitor networks.

In the network of Fig. 2.9(b), current to the right causes $Q_1$ to discharge C through diode $D_4$, after which $C_1$ charges through $D_2$ and the base-emitter junction of $Q_1$; when the current reverses, $Q_2$ discharges C through $D_3$, and C charges in the opposite direction through $D_1$ and the base-emitter junction of $Q_2$. The network of Fig. 2.9 (c) works in the same way; the use of complementary transistors allows elimination of two diodes.

Careful consideration of the single-capacitor networks reveals that if the voltage across the capacitor at the end of each switching interval is large enough and of the right polarity to forward bias the discharge diode, the analysis of the preceding section describes the operation of the circuit, except that $v_{D1} = v_{D2} = -V_o$. If, however, at some modulation level one of the pulse lengths is so short that the end-of-interval capacitor voltage is not sufficient to forward bias the discharge diode, no discharge takes place and the next charging interval begins at the charge level of the preceding interval. In this mode of operation, the longer pulse is independent of m, switching frequency increases with modulation level, and distortion is present in the modulation process.

If the parameter $r = (aIR - V_d)/V_o$ is introduced it may be shown that, for the single-capacitor networks, linear, constant-frequency operation is obtained up to a critical modulation level, given by

$$m_c = (r - 1)/(r + 1), \quad r \geq 1 \qquad . \qquad (2.54)$$

For values of $m \geq m_c$, however, the switching frequency becomes

$$f = f_0/[1 - (m - m_c)/2] \qquad , \qquad (2.55)$$

where $f_0$ is the value for $m \leq m_c$ given by (2.42) (with $V_o$ replaced by $-V_o$). The distortion introduced in the modulation process can be observed from the expression for the normalized modulator average output for $m \geq m_c$, which can be shown to be

$$\bar{v}_{ON} = (m + m_c)/[2 - (m - m_c)] \qquad . \qquad (2.56)$$

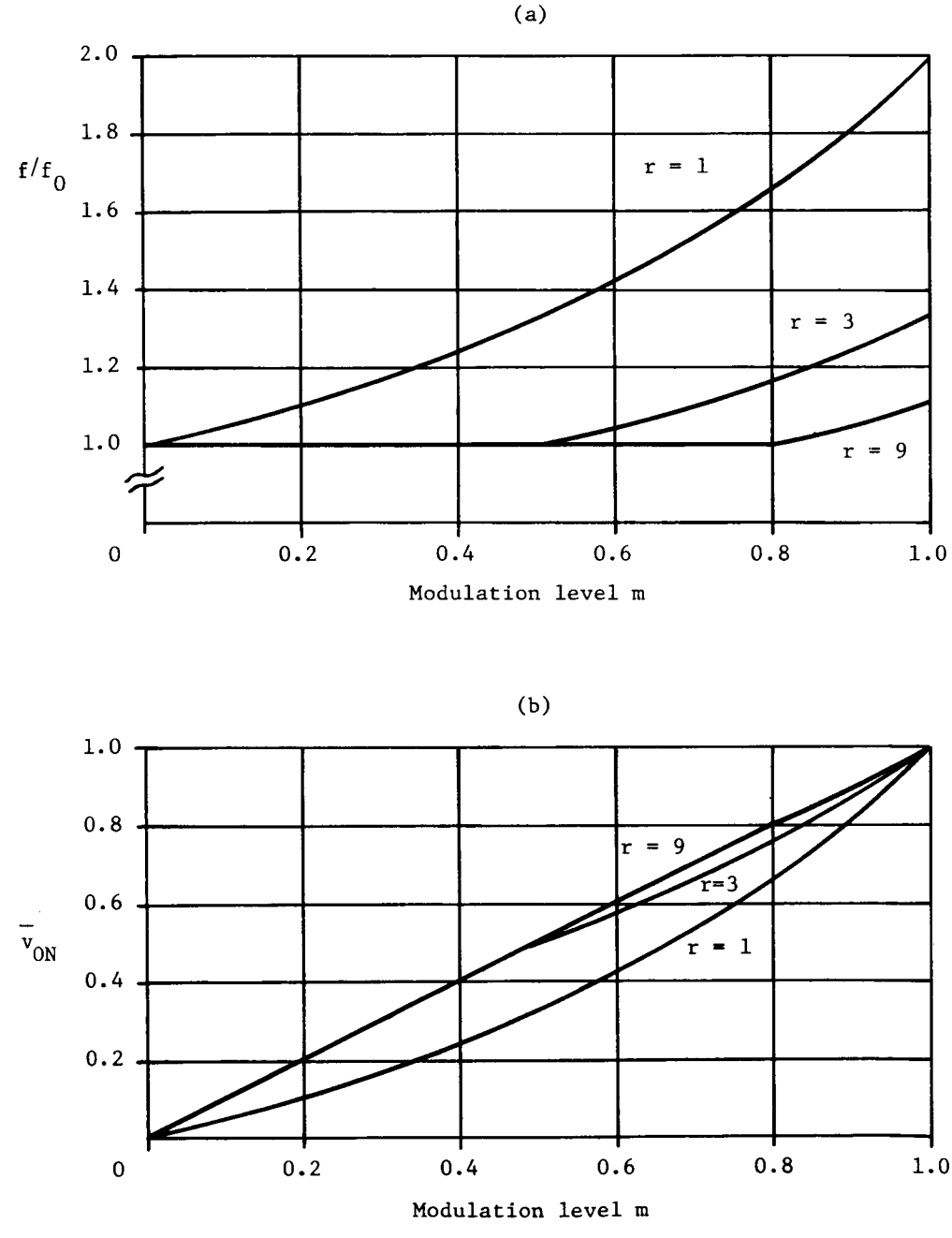



Fig. 2.10 (a) Normalized switching frequency, $f/f_0$, and (b) transfer characteristic for constant-frequency PWM design using single-capacitor switching network.

Plots of $f/f_0$ and $\bar{v}_{ON}$ versus m for several values of r are shown in Fig. 2.10. It should be observed that the frequency shift and deviation from linearity decrease as r increases. Hence, it may be concluded that the single-capacitor network, desirable for integrated-circuit realization of the modulator, yields performance that is quite satisfactory for large r ($r > 3$).

## III. Development of a Pulse-Power Amplifier

### 3.1 A basic design.

Several basic output-stage configurations for a PWM power amplifier are shown in Fig. 3.1 . Each circuit provides power to a low-impedance R-L load by alternately switching the load between equal but opposite power-supply voltages. The designs have the following elements in common:

(1) Two output transistors with similar (or complementary) characteristics,

(2) Clamp diodes, necessary for protection of the output transistors,

(3) Need for sufficient base drive to efficiently switch the output transistors.

It should be pointed out that any of the circuits shown can be connected in a bridge if only one power supply is available. For example, the basic circuit of Fig. 3.1(a), connected in a bridge configuration, is shown in Fig. 3.2 . If the supply voltage is twice V, then four times the power output for the same load can be obtained without increasing the maximum voltage across any transistor. Although there is some additional power dissipation, the bridge configuration is desirable for many space applications because only one high-current, relatively unregulated supply is required. Changes in supply amplitude do not unbalance the output, and supply ripple only slightly modulates the output.

We are interested in the selection of a circuit that exhibits performance most like that of an ideal switch, and with drive requirements that are most easily satisfied. Furthermore, the selection must be made with consideration for the design goals of high efficiency and ease of circuit integration.

The circuit of Fig. 3.1(a) offers the advantage of all-NPN design but has a significant disadvantage in that $Q_1$ is driven as an emitter follower. If it is assumed that no supplies larger than +V and -V are available, and that reactive elements may not be used, it is impossible to achieve the required drive for complete switching of $Q_1$. This means that $Q_1$ is kept well out of saturation and its dissipation at full output could be as much as 25% of the full-load power. A typical loss value for this same transistor driven hard into saturation is 8%. Failure to fully saturate one side is also likely to cause an undesirable DC offset in the output.

The circuit of Fig. 3.1(b) is similar to that just considered with one notable exception. The switching of $Q_1$ is accomplished by the switching of $Q_2$. If the $R_1 I_{B1}$ voltage drop is equal to $V_{CE(sat)}$ of $Q_2$, all drops balance and there is no DC offset in the load. However, there is significant dissipation in diode $D_1$, since it must carry the load current. This factor detracts from the usefulness of the approach for large power outputs.

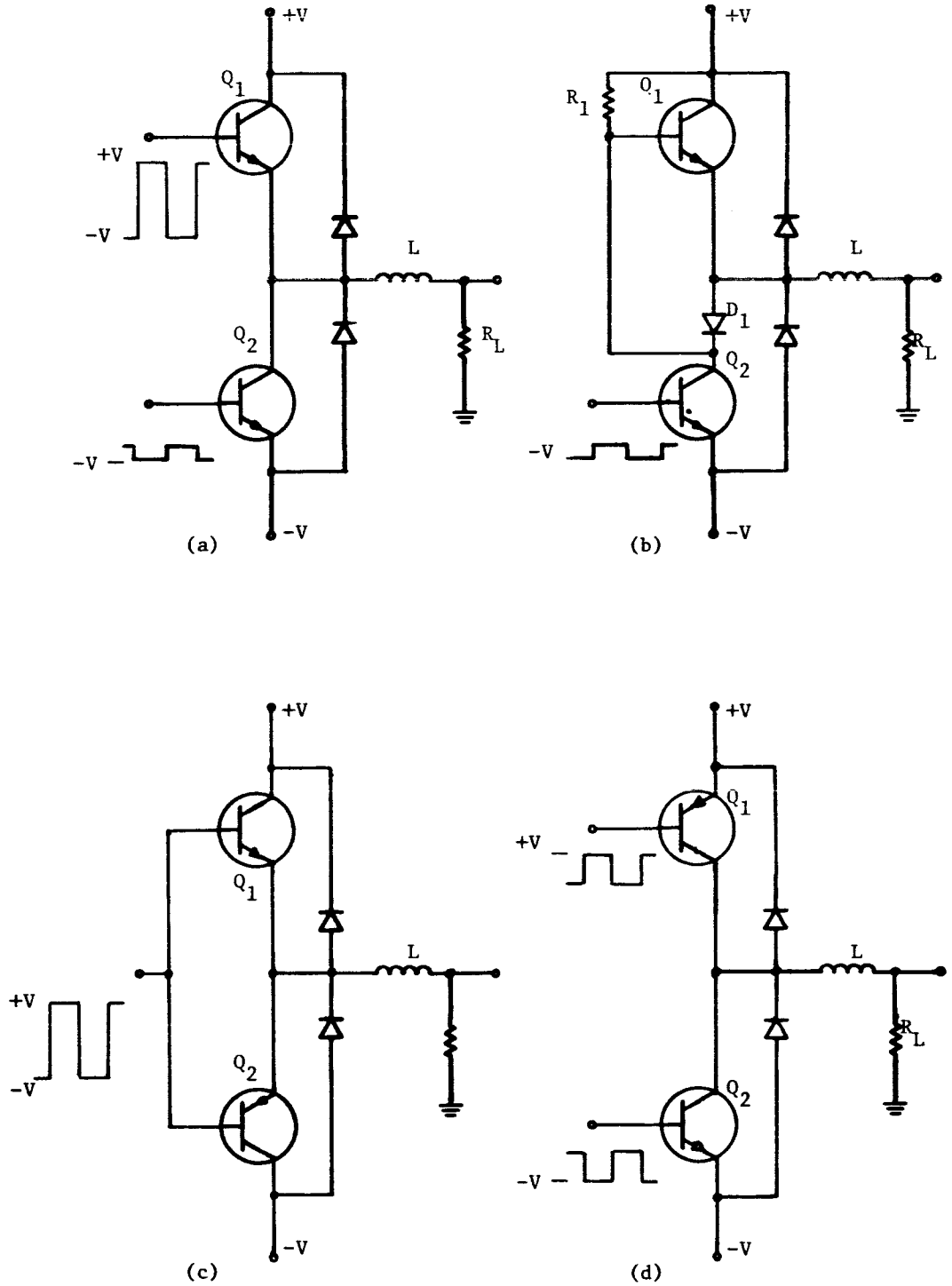



Fig. 3.1 Basic output circuit configuration

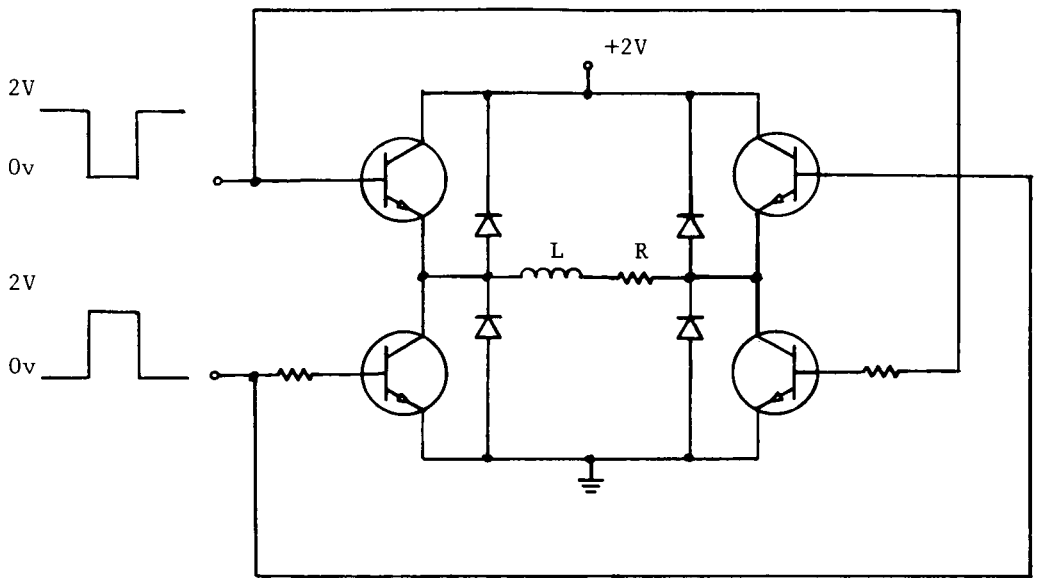



Fig. 3.2 Bridge version of the circuit of Fig. 3.1(a)

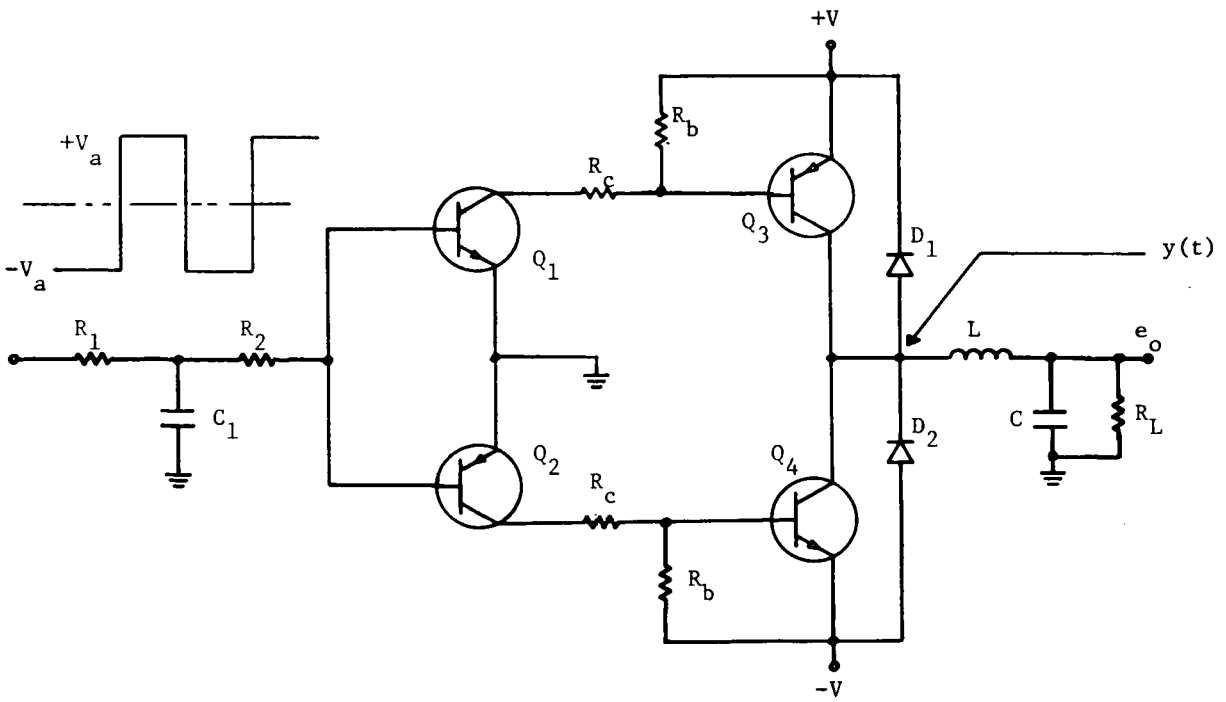



Fig. 3.3 Basic pulse-power amplifier

The dual NPN-PNP emitter-follower circuit shown in Fig. 3.1(c) suffers from the same limitations as the previous two circuits because it is both difficult to drive and has very high dissipation.

The PNP-NPN configuration of Fig. 3.1(d) represents the closest approximation to an ideal switch of the four circuits shown. Both sides are easily driven into saturation and it therefore has balanced output levels. Even when microcircuit construction is anticipated, the advantages of using complementary transistors far outweighs the increase in manufacturing difficulty. For these reasons this configuration was chosen for the output stage of the pulse-power circuit presented here.

A convenient method for driving the complementary output transistors is to employ another complementary pair as illustrated in the basic design for a pulse-power amplifier shown in Fig. 3.3 . The operation of this circuit was described in Semi-annual Report No.1, [15], and is repeated here in order that certain points may be emphasized. A PWM signal amplitude of $2V_a$ is coupled to the input through the $R_1$, $R_2$ and $C_1$ network. $R_1$ and $R_2$ limit the base drive to $Q_1$ and $Q_2$ while $C_1$ provides a slight amount of integration to help reduce switching losses in the output transistors. $Q_1$ and $Q_2$ are alternately driven between cutoff and saturation to provide the necessary base drive to the output stage. $Q_3$ and $Q_4$ alternately switch the load current unless current direction is opposite to the conducting direction of the "on" transistor. When this occurs, clamp diode $D_1$ or $D_2$ provides the path for the load current.

In order to realize the high efficiency inherent in the process of switching a transistor between cutoff and saturation, great care must be exercised in the selection of transistors, choice of switching frequency, and the details of overall circuit design.

## 3.2 Design for efficient operation.

A practical example will help in a discussion of operating efficiency. In the circuit of Fig. 3.3, $R_L$ = 50 ohms, $R_c$ = 1.2 kilohms, and $V_{cc}$ = 12 volts. If it can be assumed that the sum of transistor saturation resistance and inductor resistance is less than 5 ohms, the maximum load current will be about 200 ma. This value corresponds to a peak load-power capability of about 2 watts. Since most power amplifier applications require peak power to be supplied for only a small part of the total operating time, the power dissipation under standby (zero-input signal) conditions is of prime importance, especially for space applications. In a switching power amplifier, standby power is consumed in the following areas:

(1) Ripple power in the load,

(2) Driver-circuit power,

(3) Switching losses in the output stage.

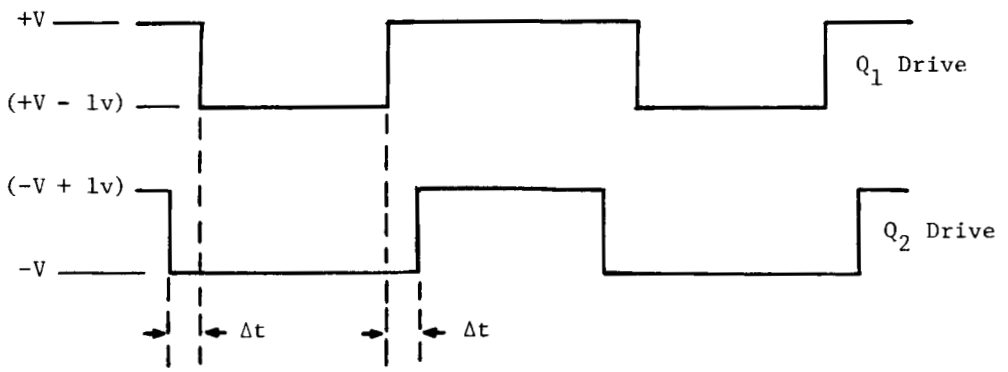



Fig. 3.4(a) Base voltage waveform for circuit of Fig. 3.1(d)

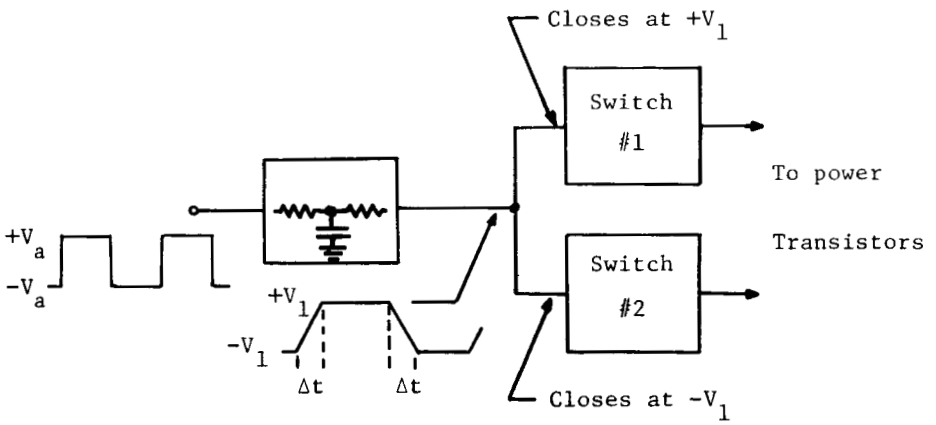



Fig. 3.4(b) Block diagram of drive waveform compensation network

Ripple power, $P_r$, is the power dissipated in the load at the switching frequency. In order to reduce $P_r$, the resistive load ($R_L$ = 50Ω) is made part of a low-pass filter. The cutoff frequency, $f_{co}$, of this filter fixes the total amplifier bandwidth, while the switching frequency, $f_0$, and the filter characteristic determine the amount of the standby power dissipated in the load. For example, without the capacitor across the load in the circuit of Fig. 3.3, the simple L-$R_L$ combination (L = 500 μh, $f_0/f_{co}$ = 5) reduces ripple power to about 100 mw. The addition of the capacitor (C = .12 μf), however, allows realization of a second-order Butterworth characteristic which reduced $P_r$ to 25 mw.

Most of the driver-circuit power, $P_d$, is dissipated in resistor $R_c$. If each of the output transistors has $h_{fe}$ = 25, for example, the base current needed to supply 200 ma to the load is about 8 ma. With allowance for the fixed voltage drops in the circuit, a value of $R_c$ = 1.2 kilohms meets this requirement. Since the base current is supplied regardless of the load demand, there is about 100 mw of standby-power loss associated with the drive circuitry. The loss is obviously reduced if the minimum $h_{fe}$ of the output transistors is higher than the 25 used in this example.

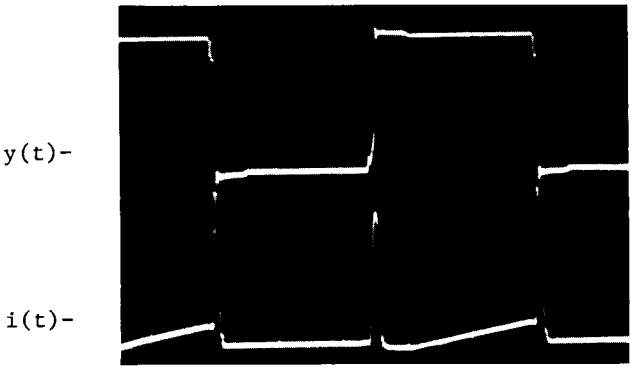
Switching losses, $P_o$, contributed by the output stage can be attributed to the following causes:

(1) Difference in turn-off and turn-on times of the output transistors,

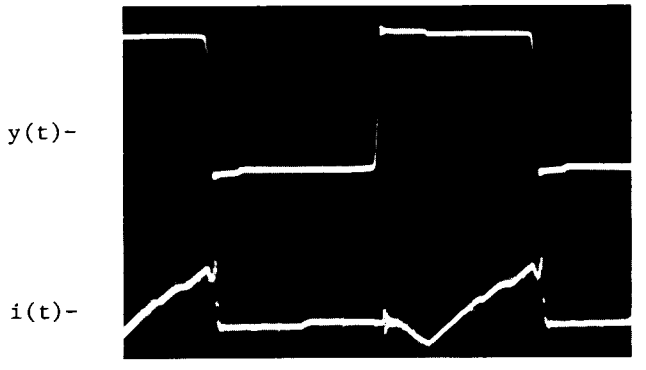
(2) Fraction of switching period spent by the transistors in their active regions,

(3) Clamp-diode conduction loss.

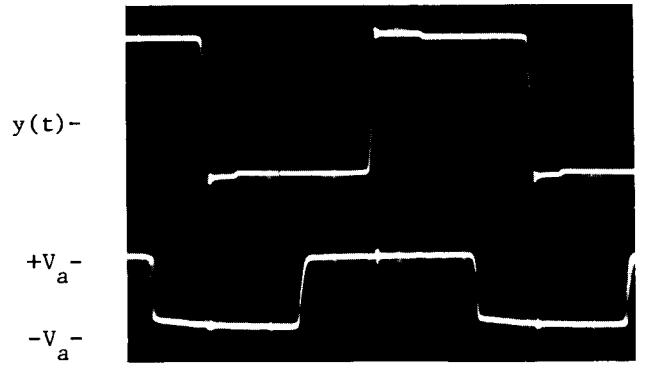
An important problem in the design of the output stage arises because the turn-off time of a power transistor may exceed the turn-on time by a significant amount [16]. This problem, caused by large storage time due to saturation, leads to very high losses that occur during switching transitions when both (or all four in the bridge), transistors may be on, which, in effect, creates an instantaneous short on the power supplies. The obvious solution involves one of creating drive waveforms which turn the "on" transistor off, before switching the "off" transistor on. Such compensating waveforms are shown in Fig. 3.4(a) for driving the circuit of 3.1(d). Here Δt should be equal to the total difference between the turn-off and turn-on times of the power transistor. These waveforms can be easily generated by a dual switch with a deadband region, preceded by an RC integration network, as in the block diagram of Fig. 3.4(b). It should be pointed out that a very large Δt will force the output into 3-state mode of operation and, although this may be desirable in rare applications, it should be avoided here. Furthermore, it should be noted that the dynamic range of the power amplifier is limited by introducing the compensation. It can be shown




(a) y(t) and Positive Supply Current; $C_1 = 0$




(b) y(t) and Positive Supply Current; $C_1 = 1680$ pf




(c) y(t) and PWM Input Signal

Fig. 3.5 Pulse-power amplifier waveforms

that the maximum modulation before the output jumps to the supply level is given by:

$$m_{(max)} = [(T - \Delta t) - \Delta t]/T = 1 - 2\Delta t/T \quad , \qquad (3.1)$$

where T is the switching period.

The simple method of eliminating momentary short-circuiting of the power supply outlined above has been utilized in the input circuit of the basic design shown in Fig. 3.3 . A look at the positive power-supply current waveform of Fig. 3.5(a), for $C_1 = 0$, shows current spikes of 400 ma which occur during switching transitions. A graphical calculation of the power loss associated with this spike, based on $V_{cc} = 12$ volts and $f_0 = 100$ kc, yields 200 mw. This loss, it should be noted, would increase linearly with frequency. The power-supply current spikes may be attenuated by adding capacitance, and, as shown in Fig. 3.5(b), are completely eliminated when $C_1 = 1680$ pf. Not only has the current spike disappeared, but the raggedness in the rise and fall of the output waveform has vanished. The drive voltage for the power stage is shown in Fig. 3.5(c). Notice that the integration network introduces a propagation delay in excess of 2 μs.

Fig. 3.6 graphically displays total standby-power loss vs. switching frequency for three values of $C_1$. The rise in losses below 50 kc is caused by the high ripple voltage across $R_L$ at low switching rates. At first glance, it appears that by choosing an $f_0$ of 70 kc, operation with $C_1 = 0$ is acceptable. The fallacy in this reasoning is that the 400 ma current spikes observed on the tested breadboard are limited in amplitude by the particular circuit impedance when the two power transistors are on simultaneously. There is no guarantee that higher amplitude spikes would not appear with other layouts and different supplies.

The switching loss associated with the time the output transistors spend in transition between cutoff and saturation depends on the choice of switching frequency. This loss may be made quite small when $f_0 = 100$ kc, by the selection of output transistors with an $f_T \geq 200$ mc, since rise and fall times are in the 100-200 ns range.

The power loss attributed to the clamp diode conduction process is also small, as can be seen by observation of the diode-current waveform of Fig. 3.7(c). With complete compensation ($C_1 = 1680$ pf), it is estimated that total switching loss of the output stage is $P_o = 25$ mw. This figure, added to $P_d = 100$mw and $P_r = 25$ mw indicates an overall standby-power loss of about 150 mw, which is in good agreement with actual measurement (see Fig. 3.6). It should be noted that the value of 150 mw represents less than 10% of the peak-power capability of the basic pulse-power amplifier.

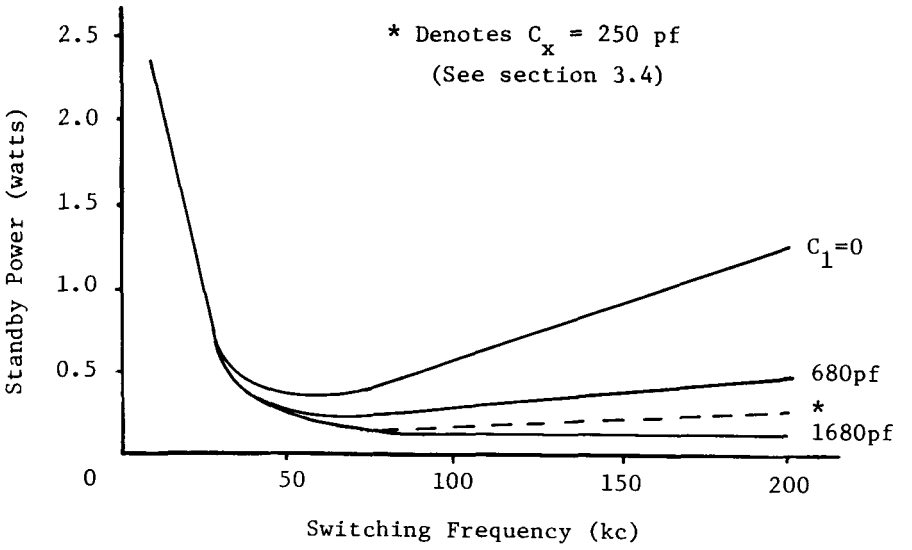


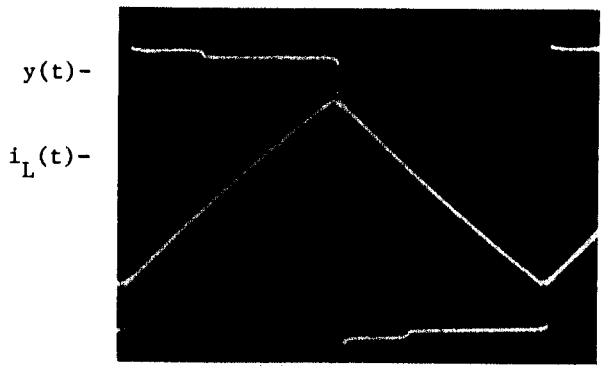

Fig. 3.6 Standby power loss

3.3 Power stage distortion.

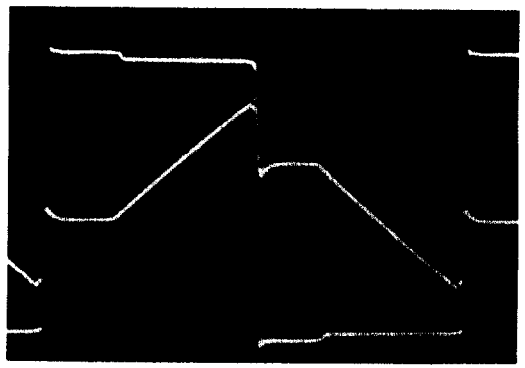
The second major area of interest when discussing pulse-power stages is the distortion introduced by circuit nonlinearities. This distortion is analagous to the cross-over distortion encountered in the design of class-B power amplifiers and should not be confused with the sideband distortion discussed in Chapter IV of this report. Consequently, distortion calculations presented here do not include either the effect of the switching frequency or spurious signals caused by the beating of input signal harmonics with the switching frequency.

3.3.1 Clamp-diode effects.

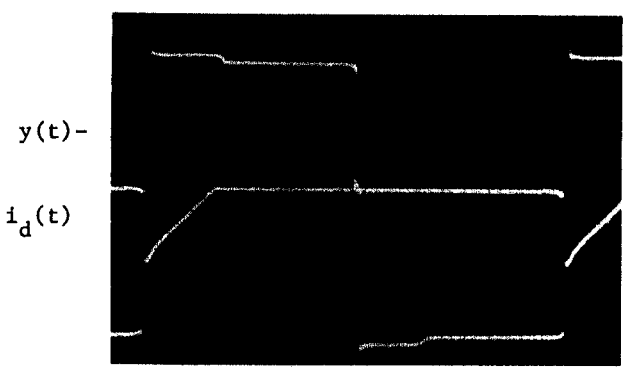
The two clamp diodes across the output limit the transistor dissipation during the time interval when the voltages on the base, emitter and collector are so polarized as to cause backward transistor action (i.e., emitter becomes collector). Inspection of the current waveforms of Fig. 3.7 shows that the diode conducts only for that part of the time when the load current exceeds the $\beta_R I_B$ backwards current in the on-biased output transistor. In the basic power stage under consideration, $I_B$ = 8 ma and, since $\beta_R$ is normally between 1 and 3, it is realistic to expect a reverse transistor current as large as 25 ma. This value is in close agreement with the picture of Fig. 3.7(b). Without a clamp diode, the voltage at the collector of $Q_1$ would rise (because of the inductor), increasing $I_B$ until $\beta_R I_B$ equaled the instantaneous ripple current. This would not only yield a high current in the transistor, but also a relatively high $V_{CE}$.



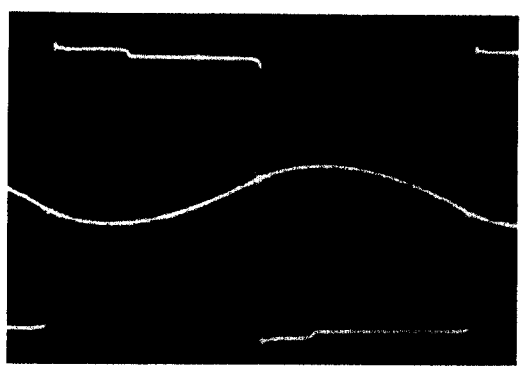

(a) y(t) and Load Ripple Current (into filter)




(b) y(t) and Transistor Collector Current




(c) y(t) and Diode Current (base line at -25 ma)




(d) y(t) and Load Ripple Current

Fig. 3.7 Power stage output current waveforms

If the load current were large, it is conceivable that transistor breakdown might occur.

For low values of modulation each transistor-diode pair operates for part of the switching cycle. As the modulation increases, the time average of the output does not change linearly because of the change in the percentage of the time that the diodes conduct. Beyond a critical value of modulation (m*), the ripple current in the load always exceeds the $\beta_R I_B$ demand of one transistor so that it never comes on in the normal conducting mode. This effect causes unbalanced output levels

$$V_1 = V_{cc} + V_d \quad , \tag{3.2}$$

$$V_2 = -(V_{cc} - V_{CE(sat)}) \quad . \tag{3.3}$$

and results in a slight increase in voltage gain for $m^*<m<1$ (see Fig. 3.8).

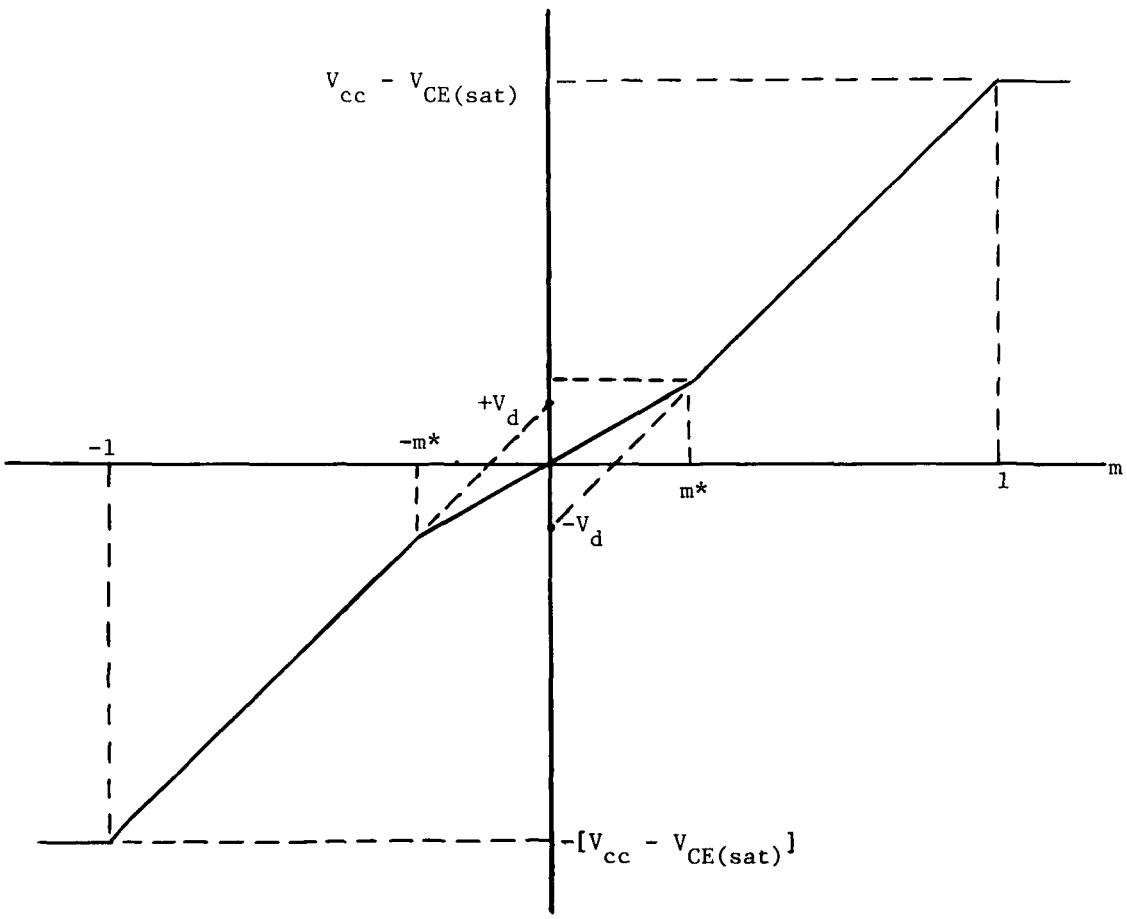



Fig. 3.8 Clamp diode effect on transfer characteristic

There are two direct solutions to the clamp-diode problem. In the first, if a voltage equal to $[V_{cc} - V_d - V_{CE(sat)}]$ could be derived for clamping, the upper clamp level would become

$$V_1 = V_{cc} - V_d - V_{CE(sat)} + V_d$$

$$= V_{cc} - V_{CE(sat)} \quad , \qquad (3.4)$$

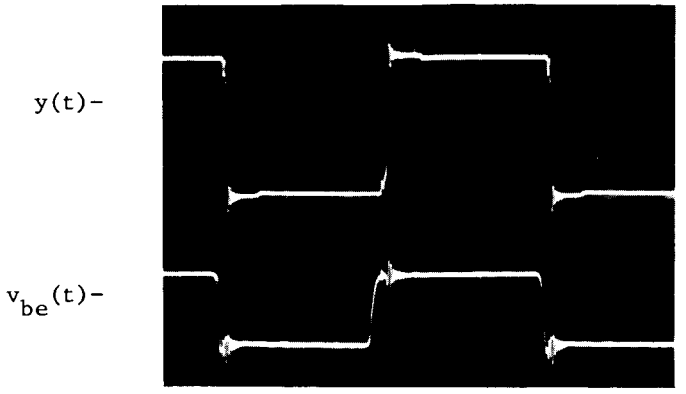
which would provide a symmetrical output waveshape (around ground) for all values of m. Unfortunately, it would take a very large amount of power to create the required clamp voltage and this solution would not normally be practical.

The second solution is to use as large a supply voltage as is practical to reduce the percentage of the output swing represented by $V_d$. For the basic amplifier where $V_{cc}$ = 12 volts, m* is 30%, and the harmonic distortion attributable to the clamp diodes, computed from the characteristic shown in Fig. 3.8 by a Fourier analysis, is 2.2% at full output.

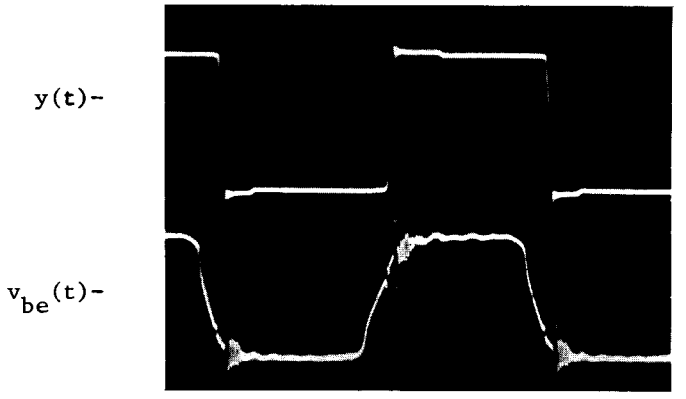
3.3.2 Distortion caused by compensation.

By far the major part of the distortion created in the power amplifier is due to capacitive effects, even in the uncompensated amplifier. Fig. 3.9 shows waveforms at the base of drive transistors $Q_1$ and $Q_2$, for $C_1$ = 0 and $C_1$ = 1680 pf. Notice that even for $C_1$ = 0, there is a slight exponential rise and fall due in part to the distributed capacitance of the breadboard and in part to the finite rise and fall time of the input-pulse generator. With $C_1$ = 1680 pf there is a considerable lengthening of rise and fall times which accomplishes the power-loss reduction mentioned in section 3.2 . The effect of increased rise and fall times on the dynamic range has already been discussed. The transfer characteristics shown in Fig. 3.10 clearly indicate that distortion increases as rise and fall times increase ($C_1$ = 0, 680 pf and 1680 pf). Notice that the slope of each of the three curves is equal for the section just above m = m*, indicating that if the two output clamp levels were equal (m* = 0), the curves would all have the same small-signal gain. Appendix A provides an analysis for m* = 0 that explains the nonlinearity of the transfer characteristics based on the exponential nature of the drive waveforms at the base of $Q_1$ and $Q_2$.

A Fourier analysis of the $C_1$ = 1680 pf curve (approximated by straight lines) was performed and the harmonic distortion for a sinusoidal input whose amplitude would cause 80% modulation was calculated to be 15.1%. This distortion might be acceptable if the power stage were to be used as a motor driver, but would certainly be objectionable for audio applications, even with a large amount of AC feedback.




(a) y(t) and $v_{be}(t)$ with $C_1 = 0$




(b) y(t) and $v_{be}(t)$ with $C_1 = 1680$ pf

Fig. 3.9 $Q_1$ and $Q_2$ base voltage waveforms

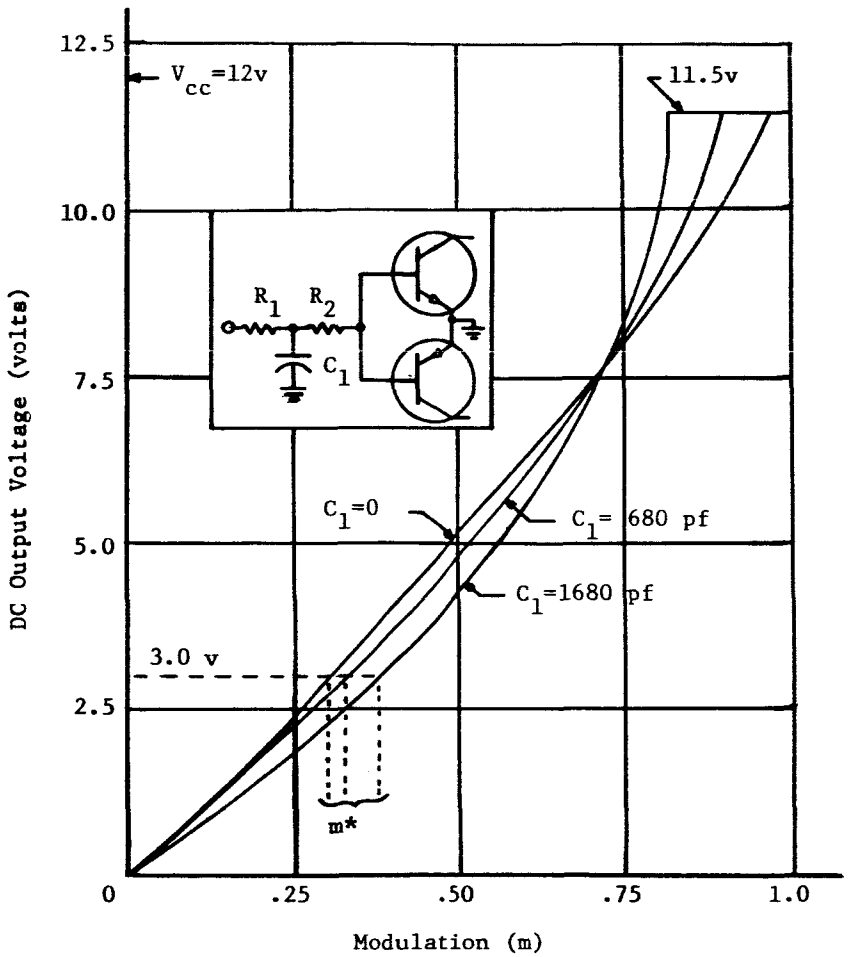



Fig. 3.10 Transfer characteristic for simple compensation

3.4 Design optimization.

There are several undesirable aspects of the compensation network presented as part of the "basic pulse-power amplifier". In addition to creating excessive distortion because of the large C necessary to reduce the switching-power loss, it causes the amplifier to be sensitive to both amplitude and DC average level of the input. This can cause an output DC offset when the input duty cycle is 50% (m = 0) which not only yields higher standby losses, but results in a non-symmetrical transfer characteristic. Furthermore, the capacitor size required (1680 pf) is beyond the desirable range for microcircuit applications.

A compensation network which alleviates these problems has been developed and evaluated and is shown with a complete power stage in Fig. 3.11 . The advantages

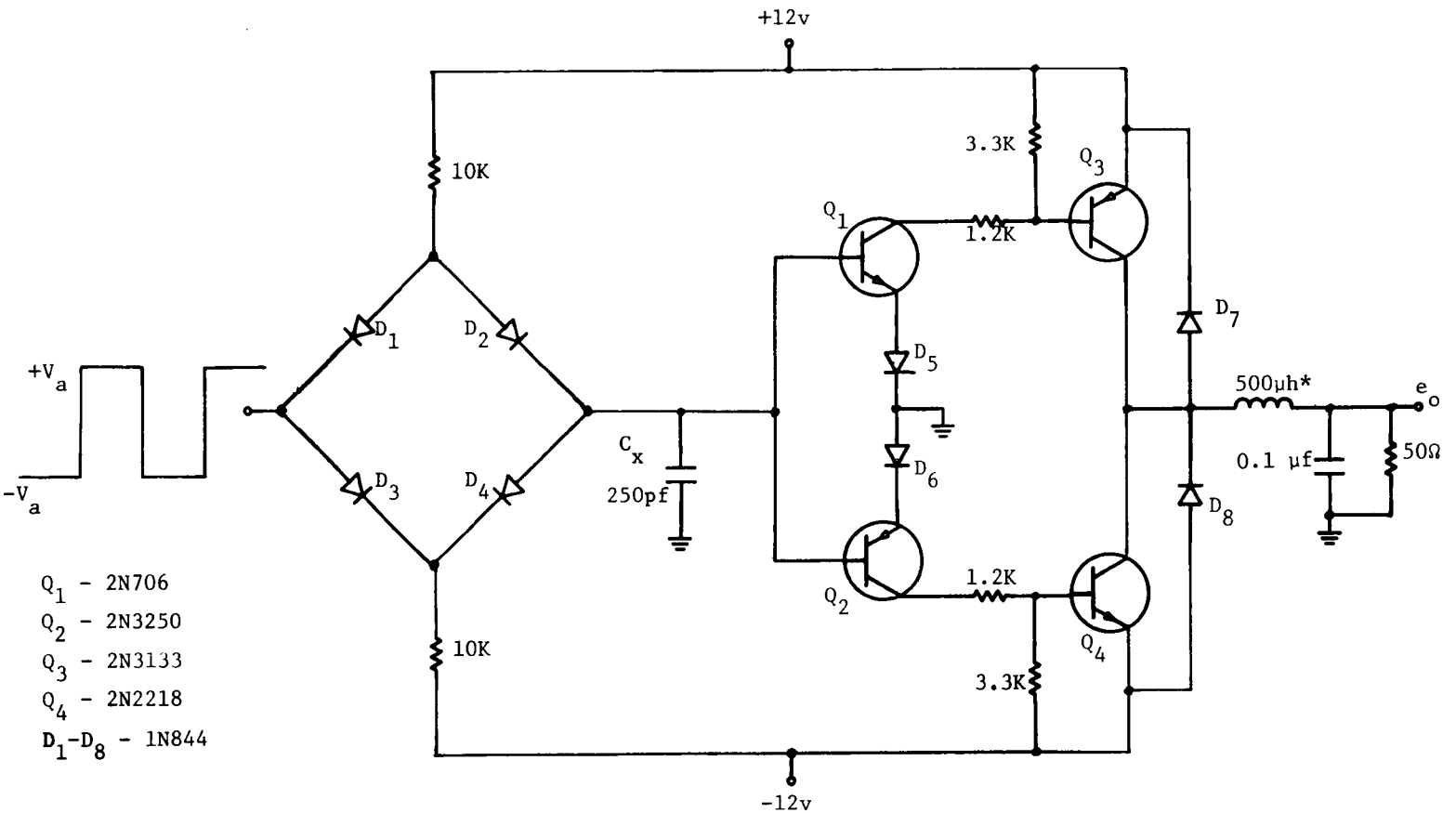



Fig. 3.11 Basic power stage with optimized compensation

of this network are:

(1) Not sensitive to input level or amplitude as long as its swing exceeds two diode drops on either side of ground,

(2) The capacitor peak voltages are clamped at two diode drops, greatly reducing the exponential effects that lead to high distortion,

(3) A smaller capacitor can be used to accomplish the required delay because of the increase in switching levels and circuit resistance.

With $C_x$ = 250 pf the power-supply spike current (see Fig. 3.5) is removed and the standby power vs. switching frequency curve is virtually the same as that for $C_1$ = 1680 pf (see Fig. 3.6).

An analysis of the limitations of this type of compensation network is continued in Appendix A. For our time constant T = 2.5 μs, switching levels of ± 1.5 volts, and for $f_0$ = 100 kc (T = 10 μs), the curve of Fig. A.4 predicts a peak modulation of m = 0.9 with linear operation up to that level. Fig. 3.12 shows an actual transfer characteristic for $C_x$ = 250 pf. Considering the fact that the analysis of Appendix A neglects the clamp-diode effects, we find very close agreement with predicted behavior.

The computed harmonic distortion for an input modulation of m = 0.9 is 4.0%, which is approximately one quarter of the distortion for $C_1$ = 1680 pf in the previous configuration, even though the degree of modulation is higher. If it is recalled that the distortion due to the clamp diodes alone is in excess of 2% for an ideal transfer characteristic, the 4.0% figure is quite realistic. Another point of interest is apparent after carefully comparing the circled points of Fig. 3.12 to the actual curve. These points were taken with $C_x$ = 0, leaving only the stray capacitance of the breadboard (including the input capacitance of $Q_1$ and $Q_2$) to provide the integration. A rough estimate of the time constant under these conditions is 0.5 μs. Applying this figure to the curve for maximum m in Appendix A, it can be seen that the computed value of m = 0.98 is within measurement accuracy of the circled points of Fig. 3.12. Finally, then, it can be concluded that the range of capacitance required for minimizing standby power causes little, if any, degradation in performance from a distortion point of view.

3.4.1 Capacitor size considerations.

In an integrated circuit, a capacitor of 250 pf requires the same chip area (approximately 500 sq. mils) as that necessary to make about 30 low-power switching transistors. The value of $C_x$ could be lowered significantly by increasing the size of the deadband between switching levels. For example, if 6V zener diodes were used in the emitters of $Q_1$ and $Q_2$ of the basic amplifier, the capacitance required would be only 50 pf. The price that is paid for this reduction is an increase to ± 6.7 volt minimum levels on the PWM input signal.

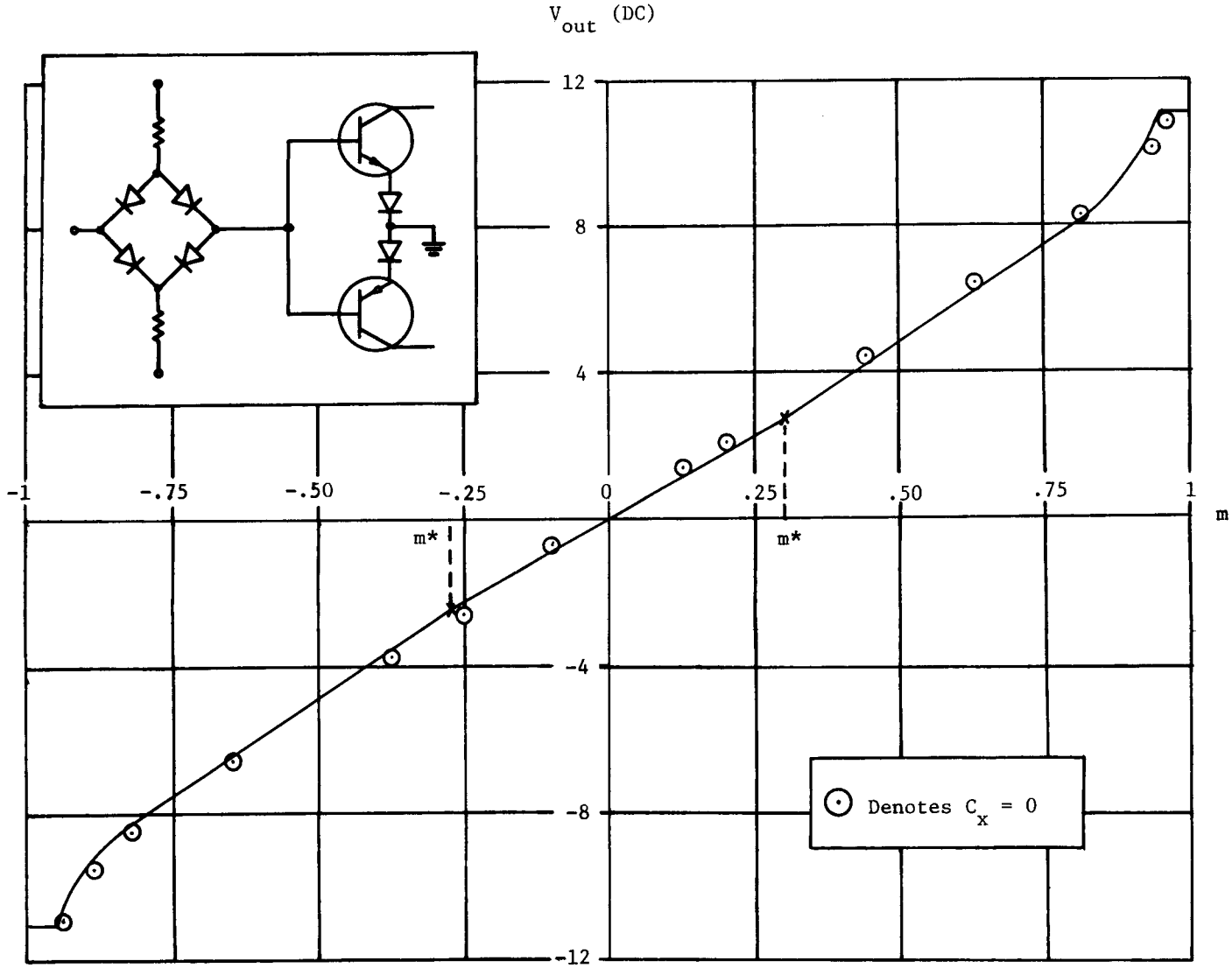



Fig. 3.12 Transfer Characteristic with optimum compensation

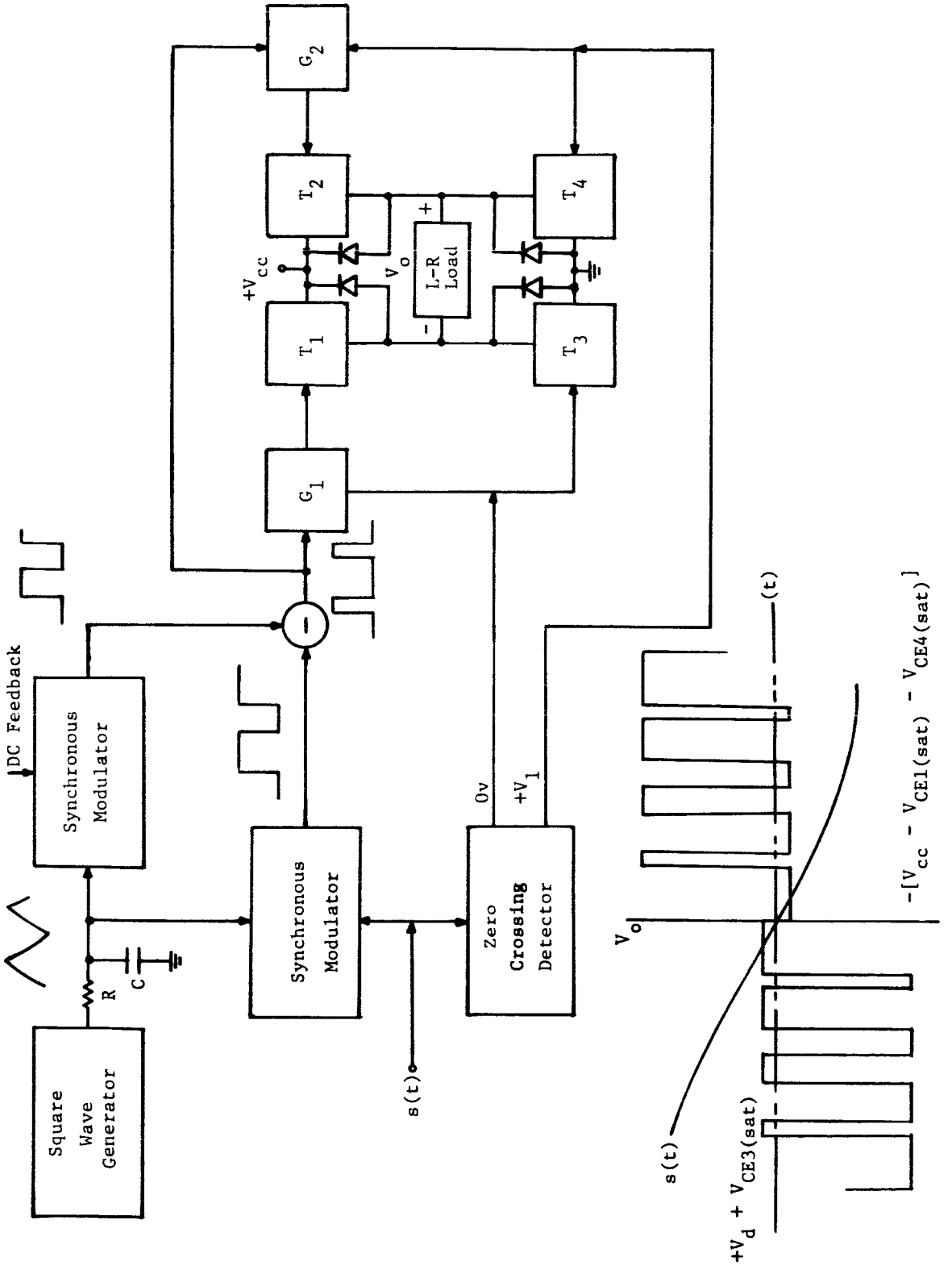



Fig. 3.13 Modified bridge output

3.5 A signal-switched bridge circuit.

As was previously mentioned the bridge output configuration is often desirable because it satisfies many system requirements. The one real difficulty in the design of this type of output is that the four power transistors must switch simultaneously. A method of modulation that permits the use of a bridge output and does not require a sophisticated compensation network approach is outlined in block form in Fig. 3.13 .

Here, the input signal, s(t), drives a zero-crossing detector in addition to a synchronous pulse-width modulator. The zero-crossing detector must have a three-state output with trigger levels balanced around ground. These levels should be small so that the output deadband is correspondingly small. If a complementary output is available from the detector, the lower pair of transistors ($T_3$ and $T_4$) in the bridge toggle at the signal rate, and are both off for the detector deadband interval. Furthermore, the detector outputs are used to drive transistor gates $G_1$ and $G_2$ which allow the modulator output to switch only one of the top transistors in the bridge ($T_1$ or $T_2$). With reference to the waveforms in Fig. 3.13, when the signal is positive, $T_4$ is "on" and gate $G_1$ is closed, permitting the modulated signal to switch $T_1$ at the higher rate. On alternate half cycles of the input, $T_3$ is "on", and the gate $G_2$, transmits the PWM signal to $T_2$.

Even though this approach to output-stage design has not been fully evaluated, it is felt that the substantial reduction in the number of simultaneous power-transistor transitions not only will eliminate the need for a compensation network, but will save enough in standby power to offset the additional circuitry required. There is obviously some crossover distortion and probably some limitation to the realizable dynamic range. Before a complete story can be told about this special bridge circuit, it must be built and checked, both analytically and experimentally, for distortion and losses.

## IV. A PWM Power Amplifier

The use of pulse-width modulation for power amplification permits the realization of the following basic criteria for space-age electronics systems:

(1) High reliability,

(2) High efficiency,

(3) Small size.

Transistors or electron tubes used in conventional audio amplifier design must be operated within their linear, active ranges. Hence, performance is quite sensitive to the effects of environmental changes and component aging. Corresponding sensitivity of a pulse-width modulation system, however, is much lower, since individual stages act as switches and performance is not degraded unless switching transistions are actually inhibited. Furthermore, the efficiency of a conventional power amplifier is limited to within a range of 30-45%, while a typical value for a switching amplifier could be in the range of 65-75%. Hence, smaller demand is made on a space-craft power supply and smaller packaging is possible because of lowered heat dissipation for comparable output levels. Implementation in silicon monolithic integrated circuit form is feasible, since procedures are the same as those employed for digital logic circuits.

It is anticipated that PWM techniques are particularly adaptable to space-craft communication, control and telemetry systems. As an interesting example of the technological advantages attainable when digital techniques are used to perform linear power amplification, consider the high-fidelity stereo system shown in the block diagram of Fig. 4.1 . In this audio system, the low-level signal from the tape recorder causes a linear pulse-width modulation of a high-frequency pulse train. The pulse train controls the switching of a pulse-amplifier stage, which in turn provides the power to drive an array of loudspeakers. Since the loudspeaker array acts as a low-pass filter, the audible output is a faithful replica of the low-level tape-recorder signal.

The PWM power amplifier used in this system is designed to deliver about 1 watt of audio power to a 50-ohm load from a low-impedance source of 0.5 volts peak-to-peak. The complete circuit, shown in Fig. 4.2, includes the simplified linear, variable-frequency modulator discussed in Chapter II and the pulse-power amplifier discussed in Chapter III. Buffering and level-shifting between modulator and the power stages are performed by transistor $Q_5$ and zener diode $Z_1$. A printed-circuit version of the amplifier, less volume control, load filter, and feedback network is shown in Fig. 4.3 . The circuit is also well-suited for realization in integrated form (see Section 4.1).

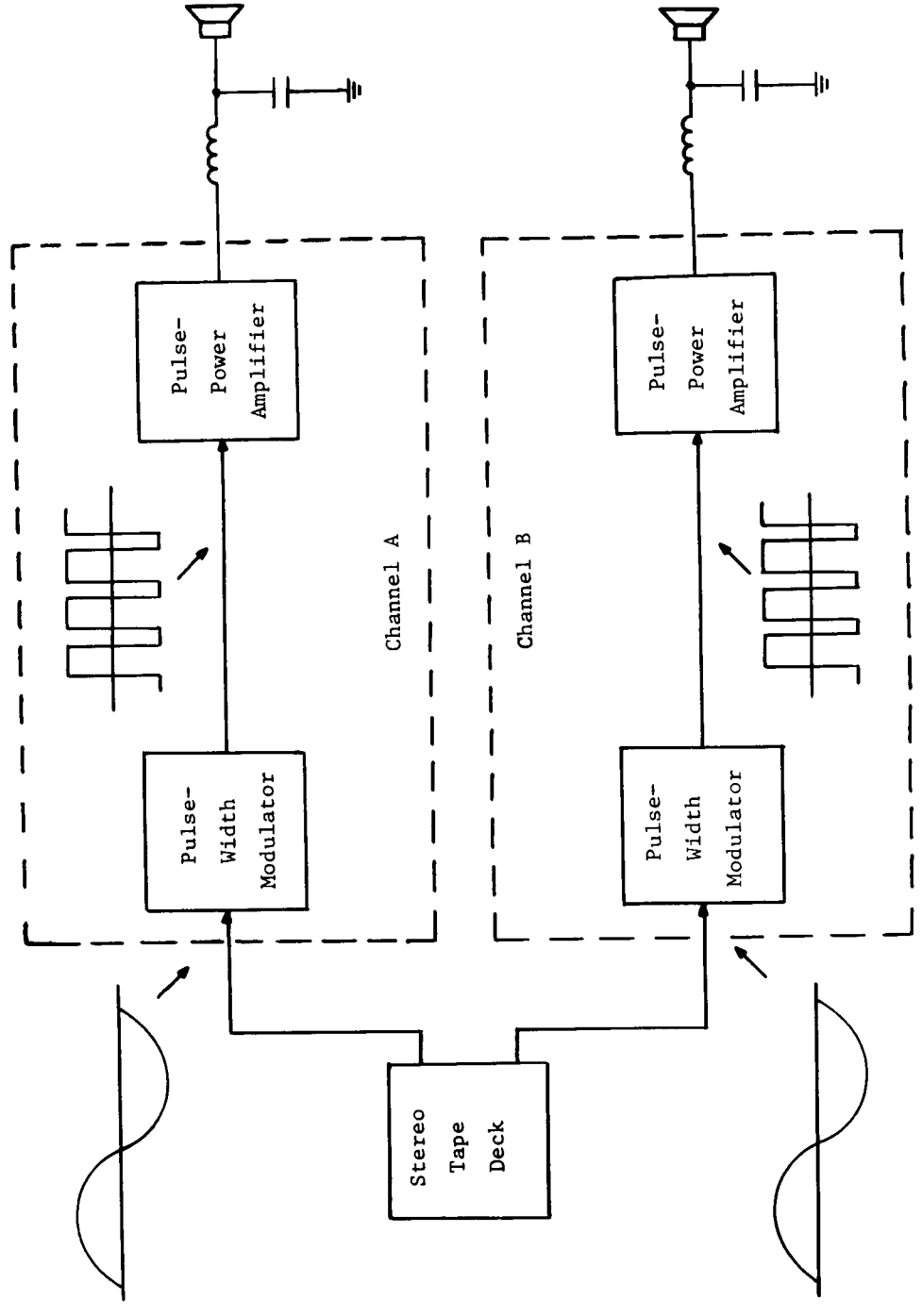



Fig. 4.1 Stereo system utilizing a PWM power amplifier

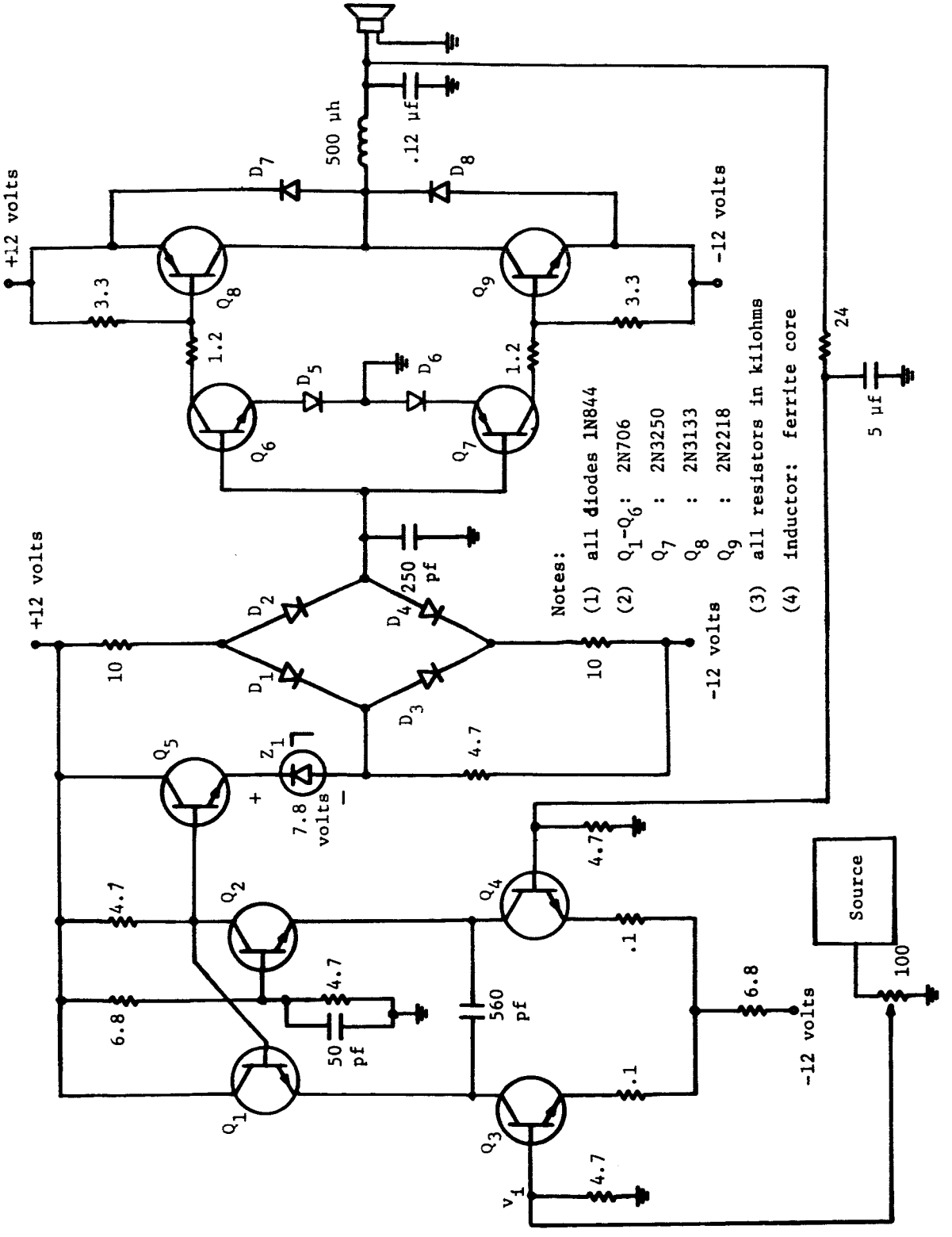



Fig. 4.2 Complete audio power-amplifier schematic

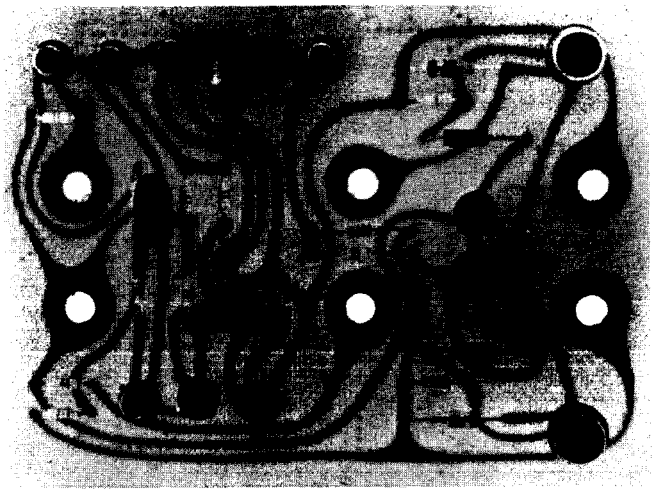


Fig. 4.3 A printed-circuit version of the PWM power amplifier

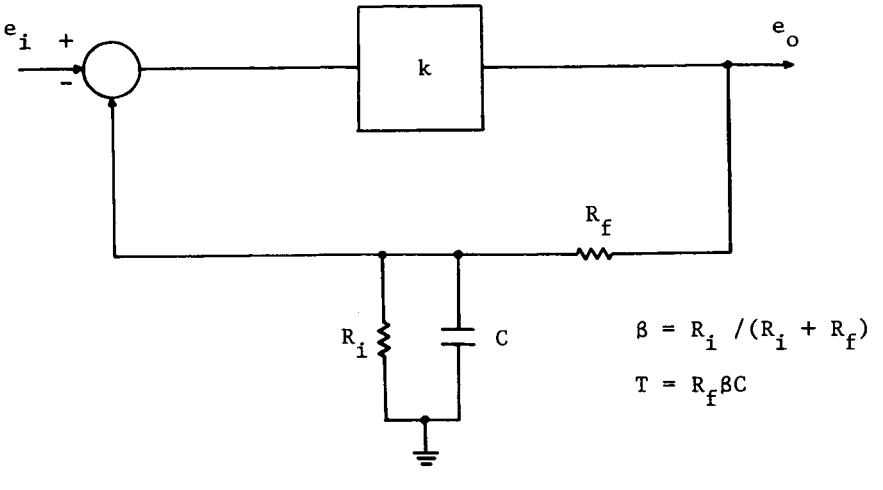



Fig. 4.4 Low-frequency model for determination of cutoff frequency

To ensure suppression of spurious harmonics that might distort the audio output, a zero-signal frequency of 100 kc was chosen. This value, along with an audio cutoff frequency of 20 kc yields a ratio $f_0/f_{co} = 5$, which has been shown to be more than adequate for suppression of this type of distortion [9, 10, 11]. It should be recalled, however, that switching frequency and modulation level are related (for the linear, variable-frequency design) by the expression

$$f = f_0(1 - m^2) \quad , \tag{4.1}$$

and therefore a value of $m = 0.9$ brings the switching frequency to the edge of the audio band. However, listening tests with audio program material containing peaks corresponding to $m = 0.9$ show no discernable intermodulation distortion. The value of $m = 0.9$ is a practical limit for another reason: the differential amplifier that controls the modulator currents becomes nonlinear beyond this level of modulation.

The low-pass filter, including the 50-ohm load is matched to a second-order Butterworth characteristic, with cutoff frequency $f_{co} = 20$ kc. The low-frequency cutoff is determined by the stabilization loop employed to reduce DC offset in the load. A low-frequency model for the amplifier is shown in Fig. 4.4, where $R_i$ is the input resistance of the differential amplifier stage, $R_f$ and C make up the feedback network, and k is the effective system gain. The proportion of the load voltage fed back, $\beta$, and the equivalent time constant, T, are defined on the diagram. It can easily be shown that the system transfer function is given by

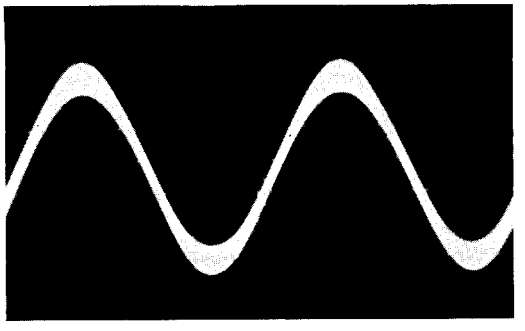
$$H(s) = [k/(1 + k\beta)][(1 + Ts)/(1 + T_1 s)] \quad , \tag{4.2}$$

where

$$T_1 = T/(1 + k\beta) \quad . \tag{4.3}$$

Hence, the low-frequency cutoff is $f_1 = 1/T_1$ and, for this system, with $k \approx 40$, $R_i \approx 3k\Omega$, $R_f = 24k\Omega$, and $C = 5\mu f$, $f_1 = 50$ cps. The amount of DC stabilization provided in this design maintains the DC offset in the load well below 100mv under normal operating conditions.

With a total standby power loss of 260 mv (about 10% of the peak power capability of the amplifier), system efficiency for a sine-wave signal at full output ($m = 0.9$) is 69%. The voltage across the load at this level of modulation is shown in Fig. 4.5(a). The blurred aspect of the waveform is due to the residue of the switching frequency riding on the signal. The effect of overdriving the amplifier is shown in

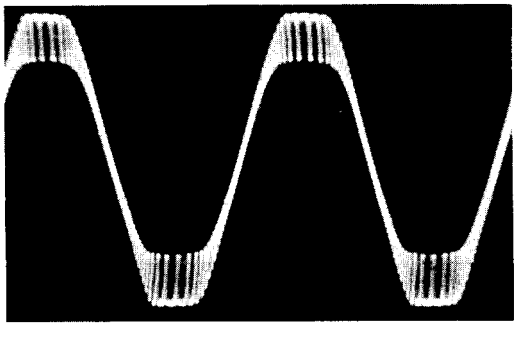


$e_o(t)$ -

- 5v/cm

- 0.5 ms/cm

(a) Load Voltage (m = 0.9)

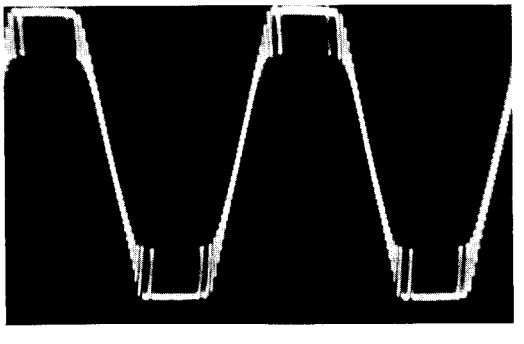


$e_o(t)$ -

- 5v/cm

- 0.5 ms/cm

(b) Load Voltage (0.9<m<1.0)



$e_o(t)$ -

- 5v/cm

- 0.5 ms/cm

(c) Load Voltage (m≃1.0)

Fig. 4.5 Load voltage waveforms ($f_s$ = 500 cps)

Fig. 4.5(b) and (c). The decrease in switching frequency with increase in modulation level can be observed. During the time associated with the flat portions of the waveform, modulator switching has ceased.

Laboratory tests of the amplifier, with a 50-ohm resistive load, yield a harmonic distortion figure of 2% for m = 0.9 (peak), which is less than what might be predicted from the discussions of Chapter II and III. It should be noted, however, that the individual modulator and power-stage transfer characteristics are complementary, i.e., they tend to compensate one another. An overall transfer characteristic is shown in Fig. 4.6(a), while a curve of harmonic distortion versus output power is given in Fig. 4.6(b). Amplifier specifications are summarized in Table 4.1 .

4.1 Microcircuit considerations.

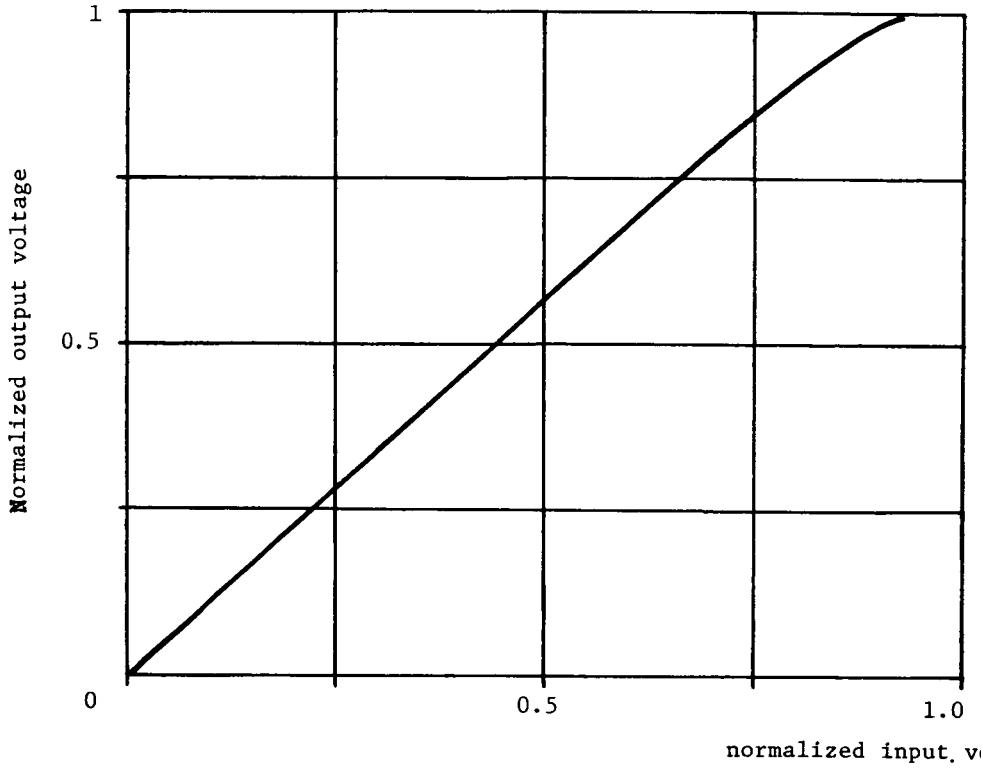
Since the amplifier presented in this chapter was designed with microcircuit limitations in mind, some discussion of possible realization in integrated form is in order here. Because two PNP transistors are used in the power stage, a dual chip layout is required. At this writing, no PNP transistors with low $V_{CE(sat)}$, high $f_T$, and high $\beta$ have been made on the same chip with comparable NPN units. As illustrated in Fig. 4.7, there would be six components on the PNP chip. These are shown within the dotted outlines on the schematic and are labeled on the chip cross-section diagram. A look at the amplifier schematic shows the PNP's cross-coupled with the two NPN's. No further amount of layout sophistication can eliminate any of the six leads necessary for interconnection of the NPN and PNP chips.

Both chips must be electrically isolated from the package because one substrate would be at -V and the other at +V. Even though this is somewhat detrimental to thermal conductivity, there should be no problem with this amplifier because the maximum dissipation (full output), on the PNP chip is 120 mw and on the NPN chip is about 180 mw. With 300 mw of total dissipation inside the package, even a free air mounting ($\theta$ = 200°C/w) would cause a junction temperature rise of only 67°C above the ambient.

When considering chip sizes it is important to eliminate certain amplifier components from consideration. The three amplifier parameters that we would like to keep control over are:

(1) Switching frequency,
(2) High-frequency cutoff,
(3) Low-frequency cutoff.

By keeping the modulator C, the feedback C, and the L-C part of the output filter outside of the package, reasonable control may be maintained. The size of the PNP chip (based on Table 3.1 of Semiannual Report No. 1) would be about 700 square mils. The



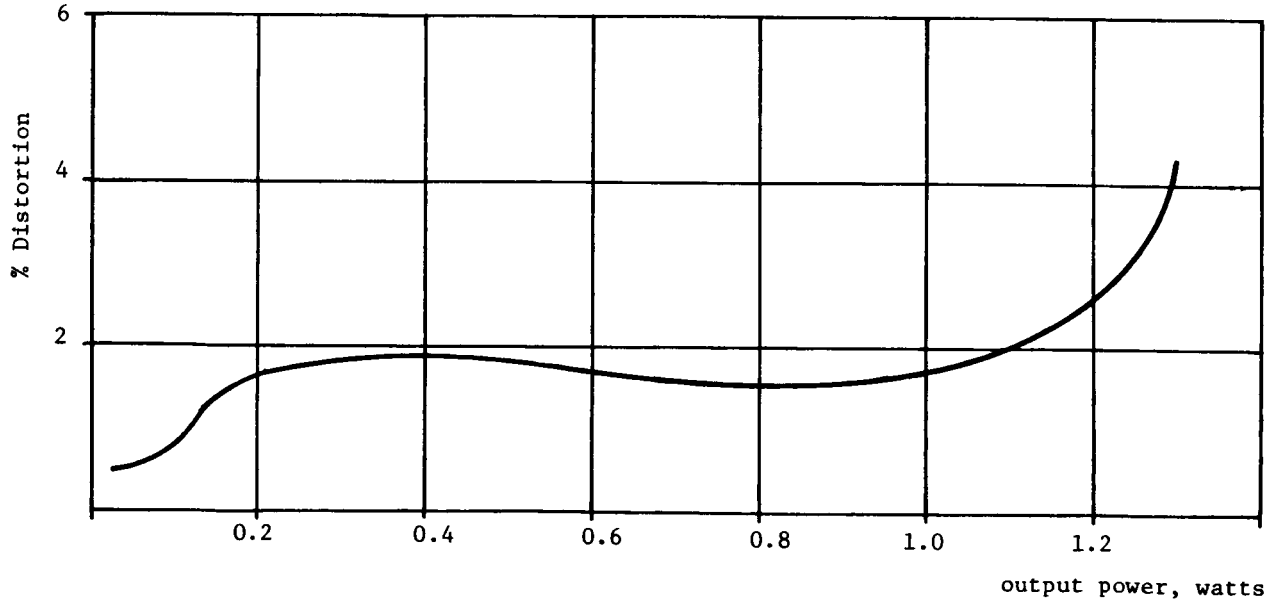
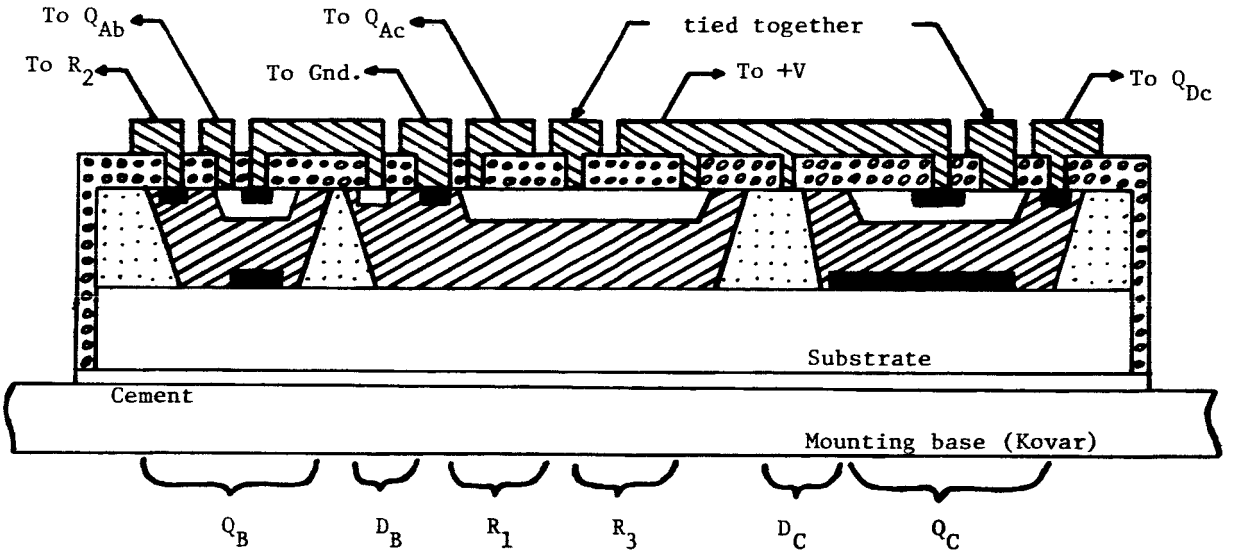




Fig. 4.6 (a) Power amplifier transfer characteristic, and (b) Curva of harmonic distortion versus power level



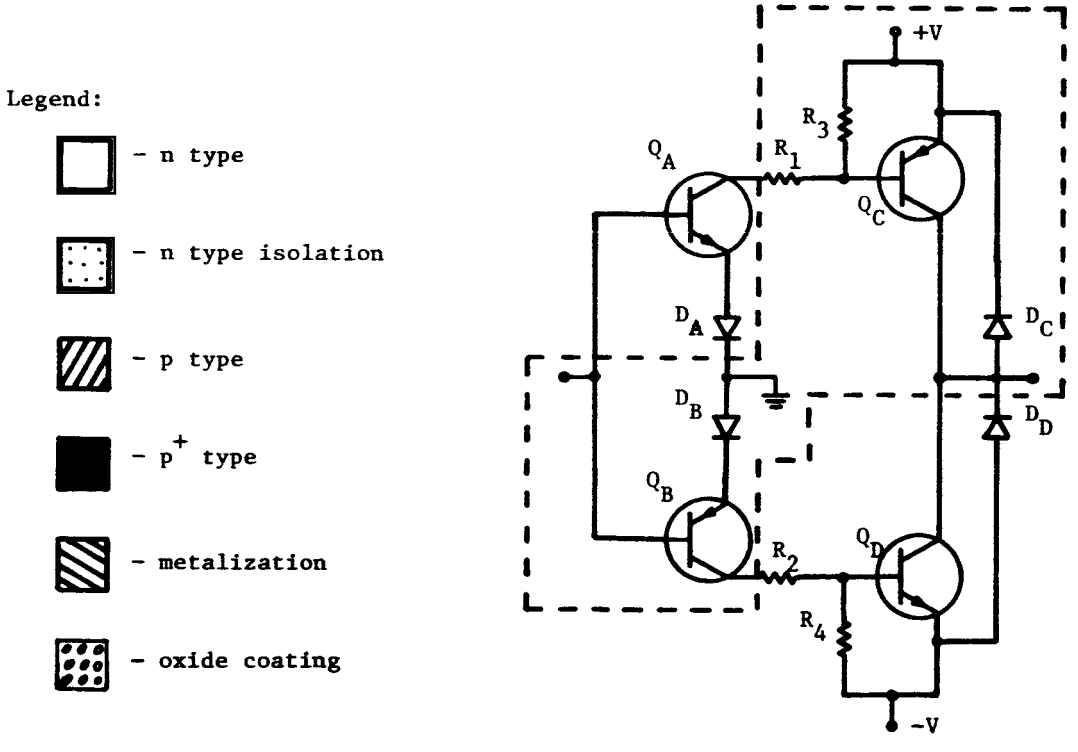




Fig. 4.7 Proposed microcircuit layout for power-amplifier PNP chip

total area required (about 2500 square mils) would easily fit in a TO-5 can or flat pack.

In summary, we feel that with some practical compromises, the amplifier appears well-suited, from every point of view, for monolithic microminiaturization.

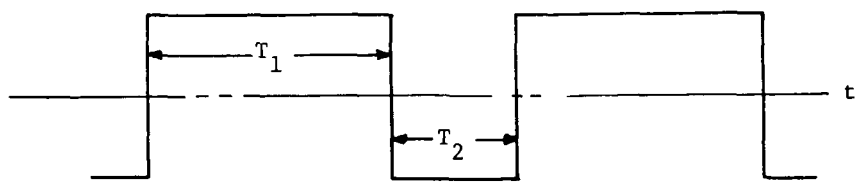
TABLE 4.1

PWM POWER AMPLIFIER SPECIFICATIONS

| | |
|---|---|
| Power supply voltage | $\pm$ 12 volts |
| Switching frequency (m = 0)* | 100 kc |
| Standby power (m = 0) | 260 mw |
| DC offset in load | 30 mv |
| Input signal for m = 0.9 | .25 volts |
| Output power for 1 kc sine wave (m = 0.9 max) | 1.28 watts |
| Efficiency at full load (m = 0.9) | 69% |
| Total harmonic distortion for 1 watt output | 2% (see Fig. 4.6(b)) |
| Frequency response ($\pm$ 3db) | 50 cps - 20 kc |

*Note: modulation level is defined:

$$m = (T_1 - T_2)/(T_1 + T_2)$$



## V. Reliability Studies

It is not uncommon for articles on passive redundancy [17, 18] to make at least passing reference to Shannon's classic paper [19] on the topic. Unfortunately, the circuit elements (or even subsystems) considered in practice rarely meet the restrictions of Shannon's idealized relay contacts. For example, the bridge array shown in Fig. 5.1(a) is a basic building block of Shannon's idealized contacts, but the bridging element of the diode analogy has uncertain significance. Direct analytic comparison is also in question, since the idealized contacts are assumed to suffer from intermittent failures only. The usual assumption for electronic components is for a permanent failure, i.e., given a failure at $t_1$, the probability that the component is still failed at $t_2$ is unity. This dependence is not included in Shannon's work.

The following analysis is essentially an extension of previous work reported by Price [20] and Hunter [21], and considers circuit elements capable of three states and uses the probability model

$$p + q + r = 1 \quad , \tag{5.1}$$

where p is the probability that the element is operating properly; q is the probability that the element has failed in a way which does not affect the operation of a composite grouping; r is the probability that the element has failed in a way which causes the entire composite to fail.

(a) (b)

Fig. 5.1 (a) Array of idealized contacts. (b) Diode analogy.

Although the composites considered here are limited to series and parallel connections, it is hoped that the techniques may be extended to include a more generalized topology. In addition, it is anticipated that the probabilistic model need not be limited to discrete modes but rather may be extended to include a continuum of performance degradation. The duality of series and parallel connections has a unifying effect on this technique, since the interpretation of q and r for one connection is interchanged for the dual.

5.1 Dual composite arrays.

Consider an element described by the probabilistic equation

$$p_o + q_o + r_o = 1 \quad , \tag{5.2}$$

and define

$$\rho_o = r_o/q_o \quad . \tag{5.3}$$

Equation (5.2) then becomes

$$p_o + (\rho_o + 1)q_o = 1 \quad . \tag{5.4}$$

Now, let $p_1$ be the probability that a composite of n such elements will operate; $q_1$ be the probability that the composite fails in a way which does not affect further composition; $r_1$ be the probability that the composite fails in a way which results in failure of additional compositions.

By definition, if an element fails in state q, the operation of the composite is unaffected. But if all the elements fail in this way, the entire composite will then be in state q. The probability of this occurrence is simply

$$q_1 = (q_o)^n \quad , \tag{5.5}$$

where n is the number of elements in the composite. Also by definition, if any element fails in state r, the composite will fail in the same way. The probability that at least one element has failed in state r may be found by subtracting from unity the probability that all elements either are operating or have failed in state q. Hence,

$$r_1 = 1 - (q_o + p_o)^n \quad . \tag{5.6}$$

Substitution from (5.2) into (5.6) yields

$$r_1 = 1 - (1 - r_o)^n \quad . \tag{5.7}$$

The probability that the composite is operating is

$$p_1 = 1 - r_1 - q_1 \quad , \tag{5.8}$$

or, from (5.5) and (5.7),

$$p_1 = (1 - r_o)^n - (q_o)^n \quad . \tag{5.9}$$

With a $\rho_1$ defined, as in (5:3), to be

$$\rho_1 = r_1/q_1 \quad , \tag{5.10}$$

substitution of (5.5) and (5.7) into (5.10) produces

$$\rho_1 = [1 - (1 - r_o)^n]/(q_o)^n \quad . \tag{5.11}$$

Rewriting equations (5.9) and (5.11) in terms of $\rho_o$ and $p_o$, we obtain

$$p_1 = [(1 + \rho_o p_o)/(1 + \rho_o)]^n - [(1 - p_o)/(1 + \rho_o)]^n \quad , \tag{5.12}$$

and

$$\rho_1 = [(1 + \rho_o)/(1 - p_o)]^n - [(1 + \rho_o p_o)/(1 - p_o)]^n \quad . \tag{5.13}$$

5.2 Series-parallel optimization.

Examination of (5.12) suggests maximization of $p_1$ with proper choice of n. By setting $\partial p_1/\partial n$ to zero, the optimum value of n may be obtained as

$$n = \ln[\ln y/\ln x]/[\ln(x/y)] \quad , \tag{5.14}$$

where $x = (1 + p_o\rho_o)/(1 + \rho_o)$ and $y = (1 - p_o)/(1 + \rho_o)$. In general, (5.14) will not yield an integral value for n, which necessitates testing the two nearest integers.

To lend further insight into the question of optimizing n, the graph of Fig.5.2 has been constructed to show bands of integral n values which satisfy (5.14) for any

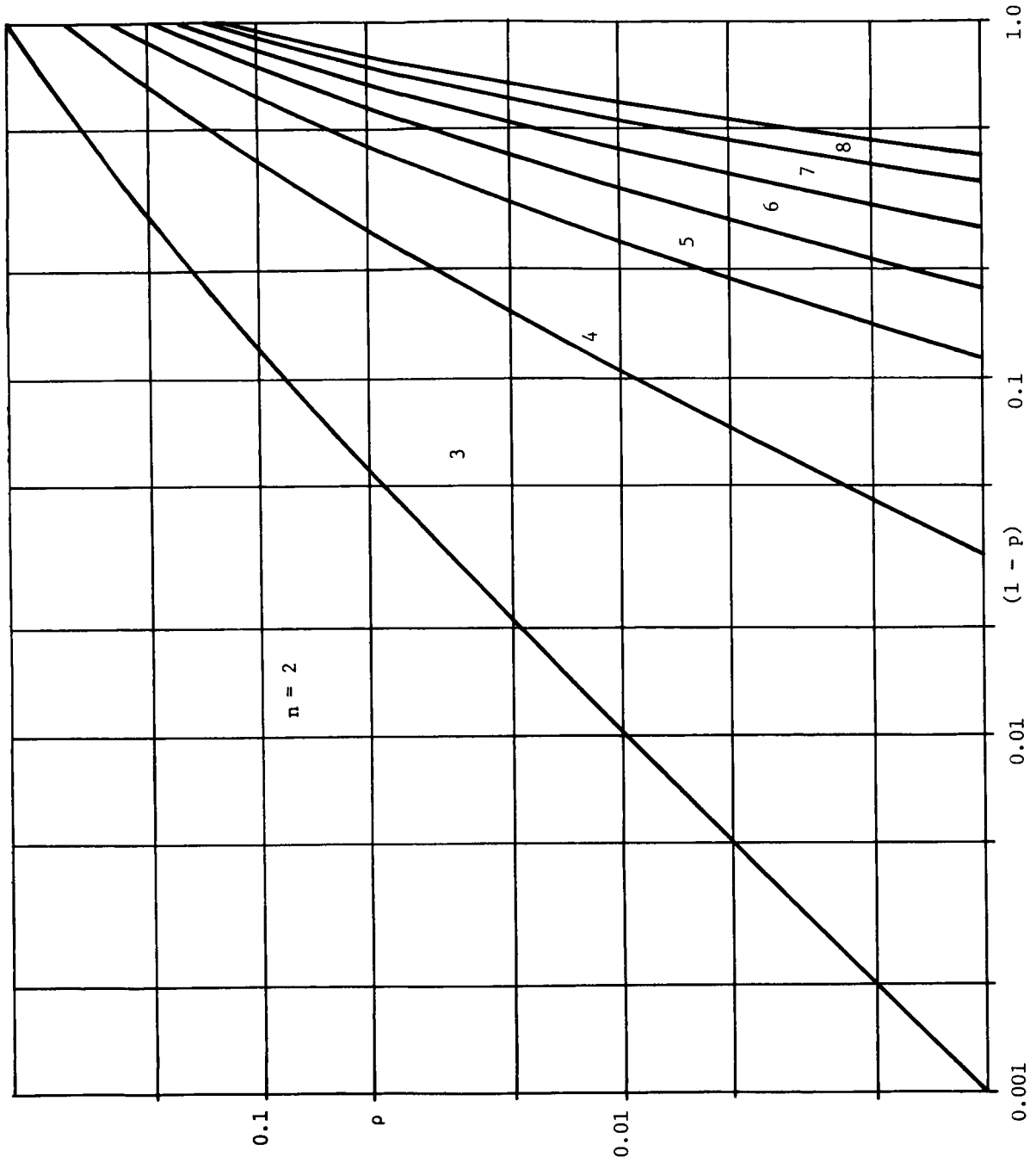



Fig. 5.2 Curves that delineate regions of optimum element redundancy

$\rho_o$ and $p_o$. Fig. 5.2 also shows that an optimum $n \neq 1$ is obtained only if $\rho_o < 1$. Analytically this can be seen by setting $n = 2$ (the minimum degree of redundancy) in (5.12), and subtracting $p_o$. Hence,

$$p_1 - p_o = [(1 + \rho_o p_o)/(1 + \rho_o)]^2 - [(1 - p_o)/(1 + \rho_o)]^2 - p_o \ ,$$

$$p_1 - p_o = p_o(1 + \rho_o p_o - p_o - \rho_o)/(\rho_o + 1) \ ,$$

$$p_1 - p_o = p_o(p_o - 1)[(\rho_o - 1)/(\rho_o + 1)] \ . \qquad (5.15)$$

For (5.15) to be positive, $0<\rho_o<1$, since $0<p_o<1$.

If a composite is formed using the optimum n obtained from (5.14), $\rho_1$ will be greater than unity. To prove this, consider a composite using optimum n with $\rho_1$ less than unity. Regardless of $p_1$, Fig. 5.2 indicates use of two such composites (total of $2n_{op}$ elements) for optimizing the operating probability. Since (5.14) has a single maximum, there is only one optimum and $\rho_1$ so chosen cannot be less than unity.

If $\rho>1$, then $r>q$ for a specific configuration. Now, if the dual configuration is considered, and the role of r and q interchanged, $r' = q$ and $q' = r$. Hence, $\rho' = 1/\rho$. Equations (5.5) through (5.15) and Fig. 5.2, now apply to the dual configuration. Each composition may be treated as a new element and some reliability improvement obtained. A typical array so synthesized is shown in Fig. 5.3 . The following numerical example illustrates the procedure.

Consider an element with operating probability $p_o = 0.5$ and $\rho_o = 0.1$ . If the criterion of (5.14) is used, the circuit of Fig. 5.4(a) is obtained, and application of (5.12) and (5.13) yields $p_1 = 0.790$ and $\rho_1 = 4.1$ . Following this arrangement by a series connection, and determining $\rho_1' = 1/\rho_1 = 0.246$, equation (5.14)(or Fig. 5.2) dictates two composites for optimum reliability. (Fig. 5.4(b)) Application of (5.12) yields $p_2 = 0.89$ .

In comparison, form the quad configuration of Fig. 5.5(b) by a composition of the parallel connection of Fig. 5.5(a). The operating probability of the parallel connection is $p_1 = 0.706$, and $\rho_1 = 0.43$, so that $\rho_1' = 2.32$ . Now, computing the operating probability of the quad arrangement, we obtain $p_2 = 0.624$! Not only is $p_2$ less than $p_1$, but it is clearly inferior to the reliability of the composite shown in Fig. 5.4(a).

5.3 Conclusions and future objectives.

The foregoing analysis sheds additional light on the practice of quad mounting certain elements for reliability improvement, and indicates that some knowledge of

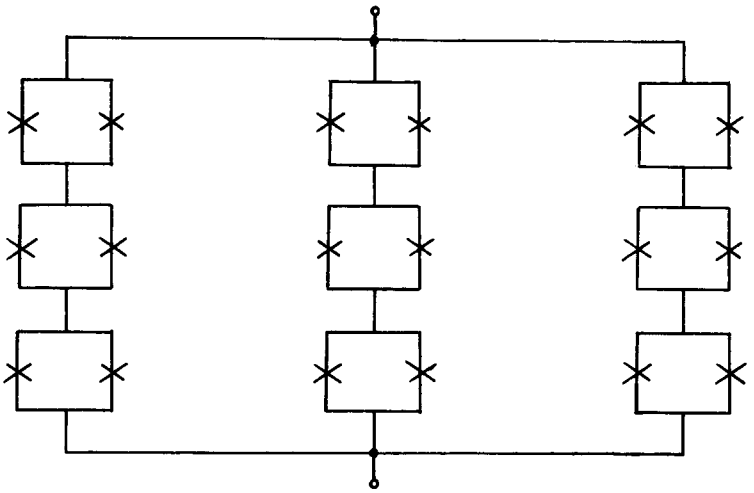


Fig. 5.3 Typical redundant element array

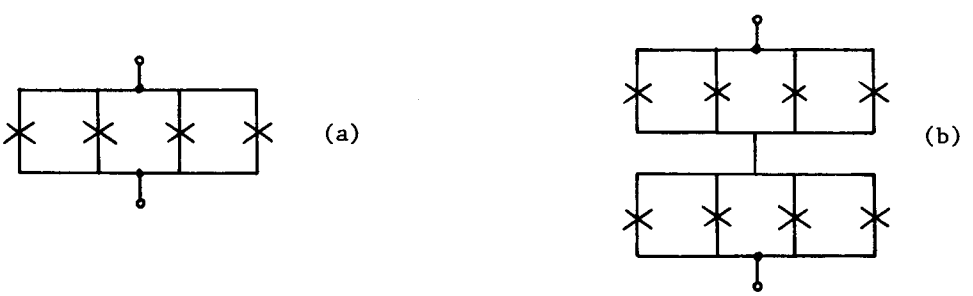



Fig. 5.4 Optimally derived array


Fig. 5.5 Common quad array

failure modes must be determined before redundancy is attempted. Fig. 5.2 does indicate however, that in the limit as $p \to 1$, the quad configuration (2 x 2) will yield some (if not optimum) improvement. Investigation of this limit is in progress.

Maximization of p for each step in a structure such as shown in Fig. 5.3 does not necessarily lead to overall optimization for total number of elements involved. However, an extension of this procedure including possible use of dynamic programming may provide an ideal topology for any desired reliability improvement.

The ultimate objective of this effort is to consider the optimum redundant arrangement of devices (including active elements) whose failure states are not catastrophic, but rather represent a continuous degradation from normal operation. Simple resistive or capacitive networks, solar-cell arrays, and amplifiers may be improved with redundancy as a result of such a study.

## VI. Conclusions and Research Plans

The research discussed in this report has been directed toward the application of advanced circuit concepts for realization of highly reliable and efficient electronic subsystems. Some of the results have posed as yet unanswered questions, which form the basis for a continuing research effort in the area of reliable solid-state circuits. The main conclusions, with suggestions for future work, are as follows:

(1) A novel scheme for linear pulse-width modulation has been presented in Chapter II and two basic circuit designs described. The first design involves modulation of capacitor-charging currents and, although switching frequency decreases with modulation level, performance is relatively insensitive to circuit variations. The second design achieves constant-frequency operation by modulation of switching levels, but requires a more complicated capacitor network. Furthermore, performance is somewhat more sensitive to variations in circuit parameters. Research will continue in the area of modulator design with special attention given to:

(a) Improvement of modulator input circuit design, including the use of FET differential amplifiers.

(b) The development of a method for interstage amplification of the modulation process.

(2) Several configurations for pulse-power amplification have been considered and a basic complementary NPN-PNP design has been evaluated (Chapter III). This configuration meets the requirement for low output impedance, since the drive necessary for saturation of the output stage may be easily provided. The problem associated with the momentary short-circuiting of the power supply that occurs if both transistors are "on" has been solved by suitable shaping of the drive waveform without compromising the linearity of the PWM process. Future plans in this area include:

(a) Developement of a high-power, single-supply, all-NPN bridge.

(b) Evaluation of an audio-switching scheme for reduction of standby-power losses.

(3) An important conclusion based on the design of the audio-power amplifier discussed in Chapter IV is that PWM techniques have great potential for technological utilization. It has been shown that such a design, combining the features of high efficiency (69%), low distortion (2%), and high reliability is entirely feasible and further, is compatable with the requirements of integrated circuit technology. It is anticipated that PWM methods are well-suited for application to spacecraft command and control electronic subsystems. Further research in this area will consist of

the following:

(a) A study of the effects of delay and ripple in the use of A.C. feedback.

(b) An appraisal of control system applications, such as servos and voltage regulators.

(4) In the area of reliability theory, a method has been presented that allows determination of reliability improvement by composition of redundant elements in series and parallel configurations. Further research in this area is planned to include:

(a) An extension of the methods presented to other topological configurations with development of reliability optimization procedures.

(b) Consideration of a probabalistic model not limited to discrete modes, that allows a representation of a continuous degradation from normal operation.

## VII. References


[1] Bedford, B. D., Improvements in and Relating to Electric Amplifying Circuits", U. K. Patent No. 389,855, March 1933.

[2] Watts, R. J., "Pulse-Width Modulation", U. S. Patent No. 2,556,457, June 1951.

[3] Birt, D. R., "Modulated Pulse A. F. Amplifiers, An Alternative Approach to the Design of Amplifiers Using Semiconductors", Wireless World, February, 1963, pp. 76-83.

[4] Johnson, K. C., "Pulse Modulated AF Amplifiers", Wireless World, March, 1963, pp. 135-136. (Published under Letters to the Editor)

[5] Cooper, George Fletcher, "Class D Amplifiers, Efficiency at a Price", Audio, June, 1963, pp. 24-30,48,50.

[6] Cooper, George Fletcher, "Class D Amplifiers, A closer look", Audio, July, 1963, Part I; August, 1963, Part II.

[7] Stark, Peter A., "Class D for Efficiency", Audio, June, 1964, Part I, pp.23-44; July, 1964, Part II, pp.24-46; August, 1964, Part III, pp.23-44.

[8] Crowhurst, Norman H., "Development of a Pulse Modulated Audio Amplifier", Audio, September, 1965, Part I, pp.19-50; October, 1965, Part II, pp.32-40; November, 1965, Part III, pp.36-73; December, 1965, Part IV.

[9] Carlson, A. W., Scientific Report No. 6, Contract No. AF19(604)-4089, May, 1961, Transistor Applications, Inc., Boston, Massachusetts.

[10] Bell, E. C., and T. Sergent, Bradford Institute of Technology, "Distortion and Power Output of Pulse Duration Modulated Amplifiers", Electronic Engineering, August, 1965, pp.540-542.

[11] Lukas, Billy F., "An Investigation of Pulse Duration Modulation", M.S. Thesis, University of Kansas, 1963. (Published under NASA No. N65-30962)

[12] Bose, A. G., "A Two-State Modulating System", Electro-Technology, August, 1964 pp.42-47.

[13] Loos, C. H., "Time Proportional Control", Control Engineering, May, 1965, pp.65-70.

[14] White, Harold V. and Herbert R. McCarley, "A Switching Mode Servo Amplifier Using Pulse-Width Modulation", April, 1965. (Published by Inertial Systems Branch, Army Inertial Guidance and Control Laboratory, Redstone Arsenal, Alabama, DA Project No. 1X279191D678, Report No. RG-TR-65-5).

[15] Bach, R. E., Jr. and A. W. Carlson, C. A. Furciniti, R. E. Scott, "Reliable Solid-State Circuits", Semiannual Report No. 1, NASA NGR-22-011-007, Northeastern University, Boston, Mass., July 1, 1965.

[16] Moll, J. L., "Large-signal Transient Response of Junction Transistors", Proc. IRE vol. 22, December, 1954.

[17] Suran, J., "Redundant Circuit Design, Payoffs and Penalties", EEE, September,1964.

[18] Teaste, R., "Digital Circuit Redundancy", IEEE Transactions of Reliability, June, 1964.

[19] Shannon, C. E. and E. F. Moore, "Reliable Circuits Using Less Reliable Relays", Journal of the Franklin Institute, September, 1965.

[20] Price, H. W., "Reliability of Parallel Electronic Components", IRE Transactions of Reliability, April, 1960.

[21] Hunter, L. C. and R. E. Barlow, "Criteria for Determining Optimum Redundancy", IRE Transactions on Reliability, April, 1960.

## APPENDIX A

### Nonlinearity in a PWM Amplifier Introduced by an R-C Compensation Network

The addition of an R-C network to the front end of the pulse-power stage of a PWM power amplifier effectively shapes the PWM waveform. Proper shaping avoids momentary shorting of the power supply in the output stage, as discussed in Chapter III. This process, however, has some adverse effects on the amplifier transfer characteristic. In the following analysis, in each of the two cases considered, the PWM drive signal is assumed to have voltage levels $\pm$ V, constant period T, with individual pulse lengths given by

$$T_1 = T(1 + m)/2 \quad , \tag{A.1}$$

$$T_2 = T(1 - m)/2 \quad , \tag{A.2}$$

where m is the modulation level.

A.1 Finite load impedance-perfect switch.

Consider the R-C compensation network and switching arrangement shown in Fig. A.1(a). The analysis of this case is simplified if the $V_{BE}$ drops of transistors $Q_1$ and $Q_2$ are assumed to be zero. Hence, switching action is initiated by a polarity reversal of the voltage across the capacitor. It is also assumed that resistor $R_2$ is large compared with the input impedance of transistors $Q_1$ and $Q_2$. An equivalent input circuit for this case is shown in Fig. A.1(b), along with waveforms for the equivalent PWM input, $x_e(t)$, the capacitor voltage $V_C$, and the power-switch output, y(t).

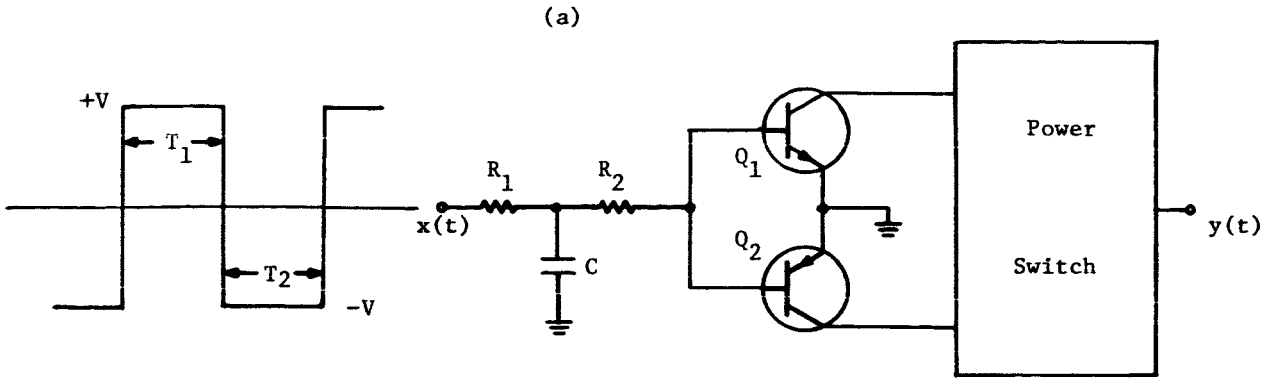
If $t_1$ and $t_2$ are defined as the times during intervals $T_1$ and $T_2$, respectively, the expressions for the voltage across the capacitor are:

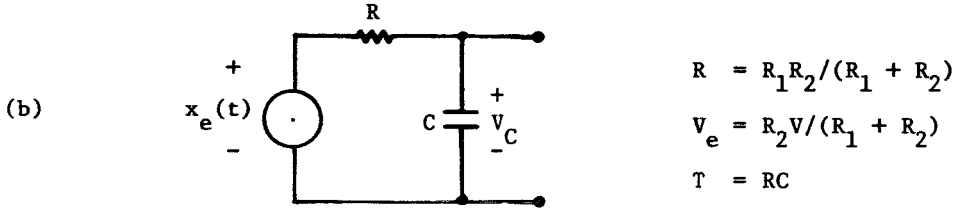
$$V_C = V_e[1 - (1 + A)\varepsilon^{-t_1/T}], \quad 0 \leq t_1 \leq T_1 \quad ; \tag{A.3}$$

$$V_C = -V_e[1 - (1 + B)\varepsilon^{-t_2/T}], \quad 0 \leq t_2 \leq T_2 \quad , \tag{A.4}$$

for the two time intervals shown. If steady state conditions prevail, parameters A and B are given by

$$A = (1 - 2\varepsilon^{-T_2/T} + \varepsilon^{-T/T})/(1 - \varepsilon^{T/T}) \quad ; \tag{A.5}$$



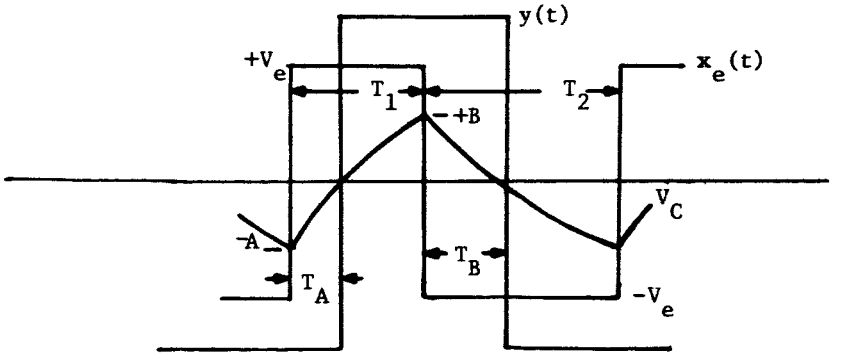




Fig. A.1 (a) Power switch with R-C compensation network.
(b) Equivalent input network and waveforms.

and

$$B = (1 - 2\varepsilon^{-T_1/T} + \varepsilon^{-T/T})/(1 - \varepsilon^{-T/T}) \quad . \qquad (A.6)$$

With reference to Fig. A.1(b), during the interval $T_1$, $V_C$ is positive when $t_1 \geq T_A$, where, from (A.3),

$$T_A = T \ln(1 + A) \quad . \qquad (A.7)$$

Similarly, during the interval $T_2$, $V_C$ is negative when $t_2 \geq T_B$, where, from (A.4),

$$T_B = T \ln(1 + B) \quad . \qquad (A.8)$$

Thus, the output of the switching circuit is positive during the interval:

$$T_P = T_1 - T_A + T_B \quad , \qquad (A.9)$$

and is negative in the interval

$$T_N = T_2 - T_B + T_A \quad . \qquad (A.10)$$

Now, if we define the normalized average output signal as

$$Y = (T_P - T_N)/(T_P + T_N) \quad , \qquad (A.11)$$

substitution from (A.9) and (A.10) yields

$$Y = (T_1 - T_2)/T + 2(T_B - T_A)/T \quad . \qquad (A.12)$$

Further substitution from (A.1), (A.2), (A.7), and (A.8) results in

$$Y = m + (2T/T) \ln [(1 + B)/(1 + A)] \quad , \qquad (A.13)$$

and finally, from (A.5) and (A.6),

$$Y = m + [2T/T] \ln [(1 - e^{-(1+m)T/2T})/(1 - e^{-(1-m)T/2T})] \quad , \qquad (A.14)$$

A family of curves for Y vs m as a function of T/T is plotted in Fig. A.2 . The effects of the R-C network are apparent as a reduced dynamic range and a nonlinear

transfer characteristic. Note that when m exceeds a critical value, $m_1$, Y = 1. This critical value of m is that which makes either A or B (in (A.5) or (A.6)) negative, causing the output switch to stay in one state. The magnitude of m for which this occurs is the same whether A or B is considered and is found from (A.1) and (A.4) or (A.2) and (A.5) to be

$$m_1 = 1 - [2T/T] \ln [2/(1 + e^{-T/T})] \quad . \qquad (A.15)$$

The curve for $m_1$ as a function of T/T is shown in Fig. A.4 .

A.2 Performance with deadband and a large input impedance.

If the compensation-network capacitor is placed from the base of $Q_1$ and $Q_2$ to ground (i.e. $R_2 = 0$), $V_C$ is clamped to $\pm (V_{BE} + V_d)$. This configuration and the new definitions for $T_A$ and $T_B$ are shown in Fig. A.2 . It is assumed here that the input impedance of $Q_1$ and $Q_2$ is high compared to resistor R.

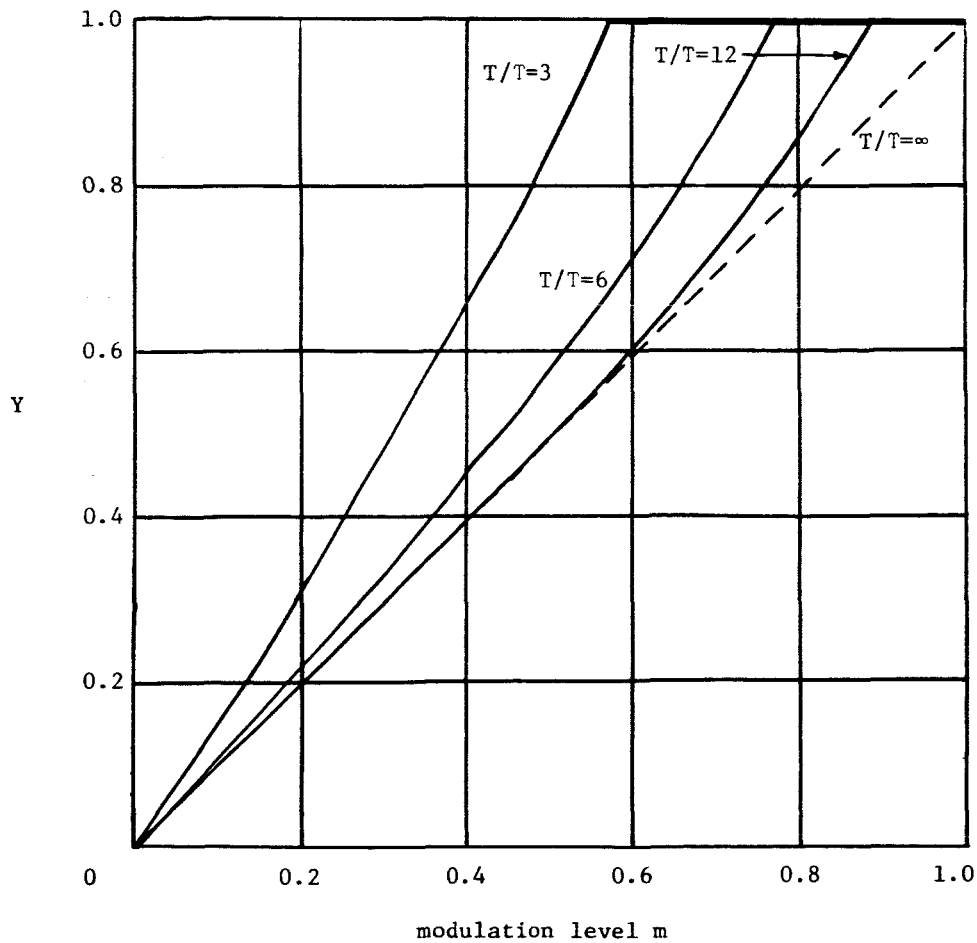



Fig. A.2 Y vs m as a function of T/T

In Fig. A.3, $T_A$ and $T_B$ are the dead-band transition times, which are

$$T_A = T_B = T \ln\{1 + (V_{BE} + V_d)/V]/[1 - (V_{BE} + V_d)/V]\} \quad . \tag{A.16}$$

An analysis similar to that presented in the previous section indicates that the transfer characteristic is linear up to the point where $T_1 = T_A$ or $T_2 = T_B$. Beyond this level the output jumps to the supply voltage because switching action ceases. If $m_2$ is defined as the input modulation level necessary to just cause Y = 1, the equation describing $m_2$ as a function of T, $(V_{BE} + V_d)$ and V is easily obtained as:

$$m_2 = 1 - (2/T) \ln\{[1 + (V_{BE} + V_d)/V]/[1 - (V_{BE} + V_d)/V]\} \quad . \tag{A.17}$$

A plot of $m_2$ as a function of T/T for $(V_{BE} + V_d)/V = 0.1$ is shown in Fig. A.4 for comparison with $m_1$.

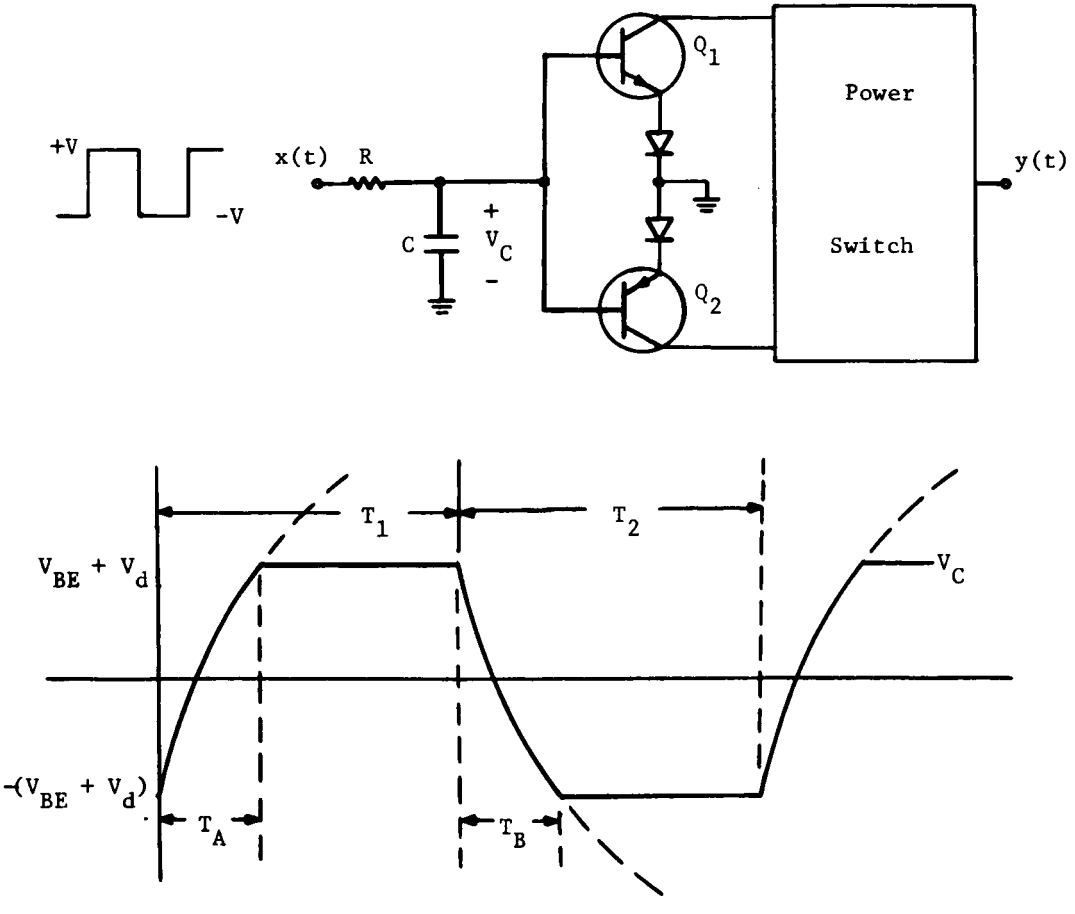



Fig. A.3 Modified compensation network

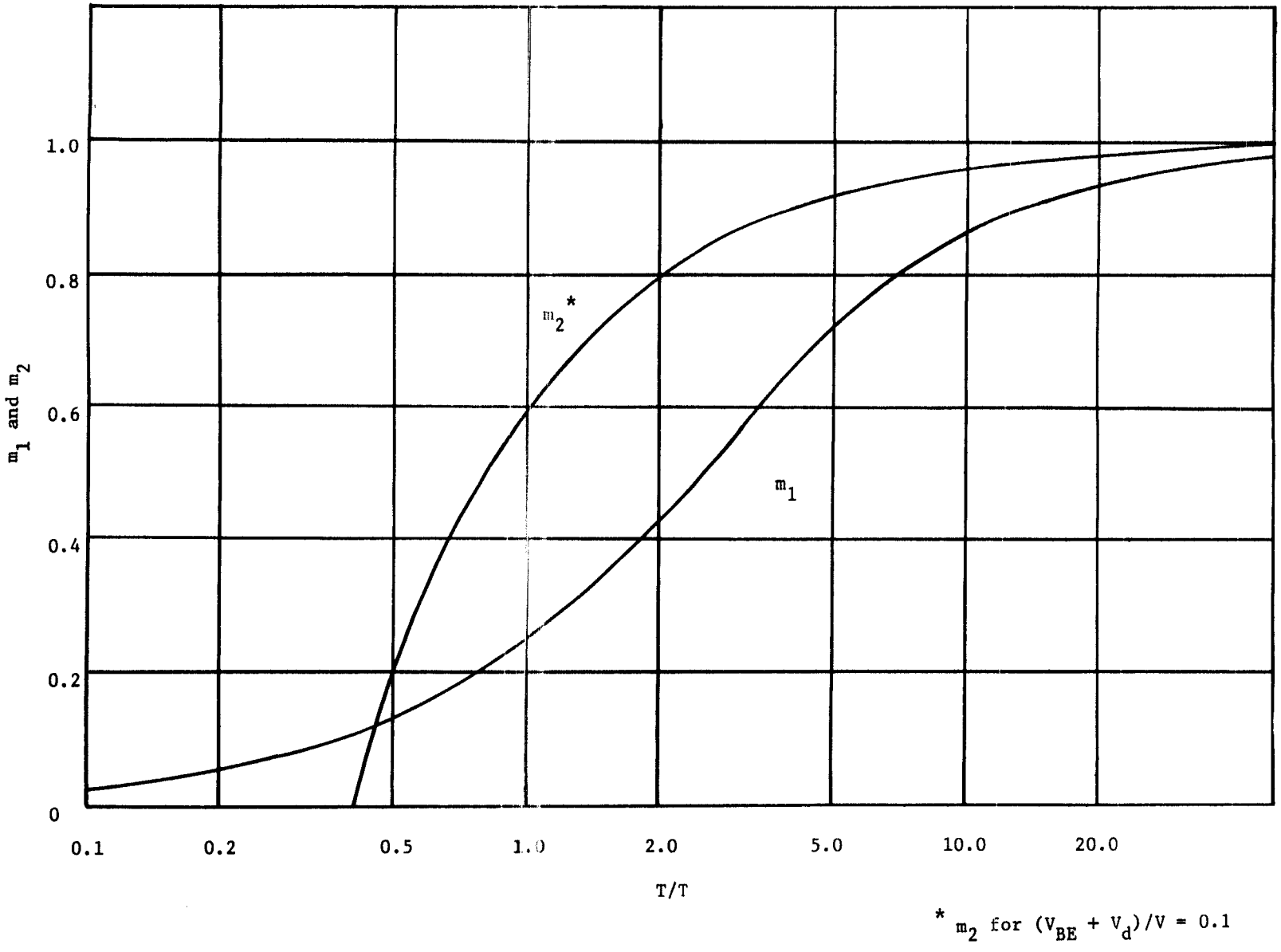



Fig. A.4 Critical modulation levels as a function of T/T